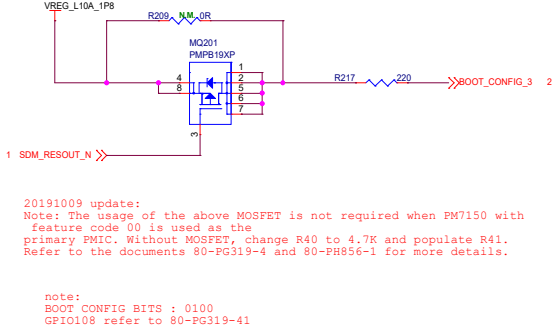
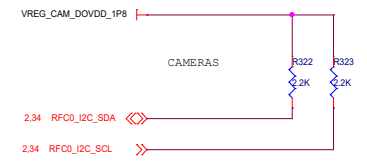
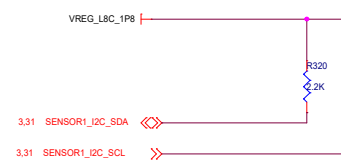
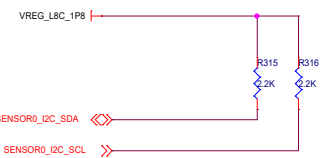
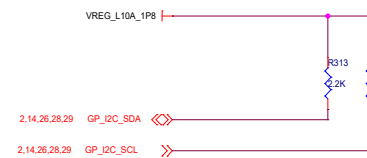
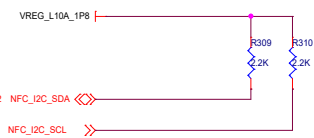
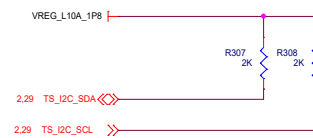
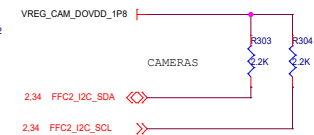
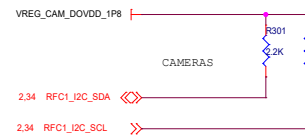
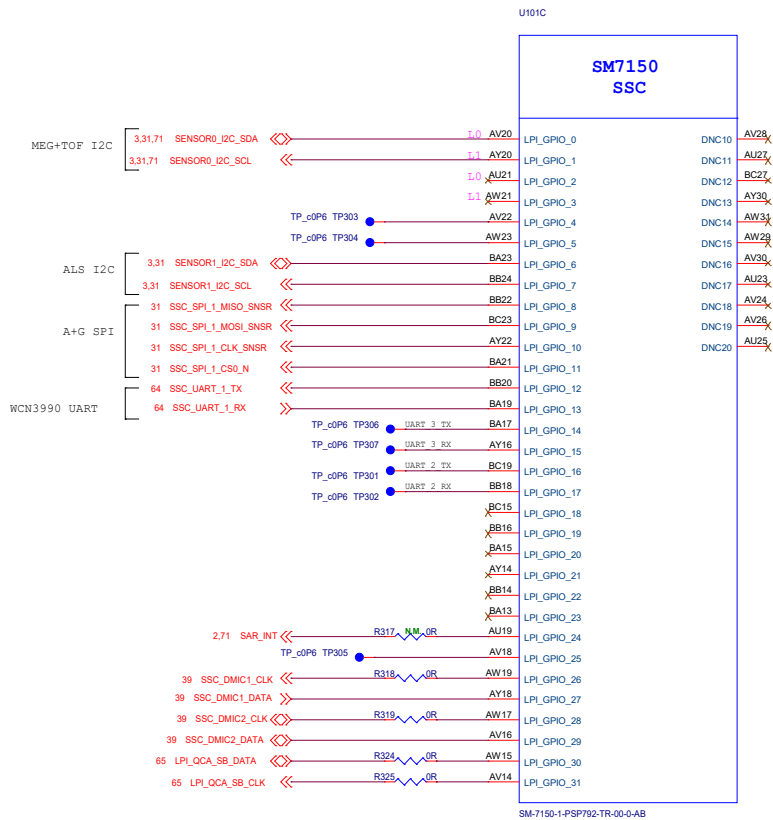


GPIO74	BOOT_CONFIG(0)	WDG_DISABLE
GPIO72	BOOT_CONFIG(1)	FASTBOOT_SEL(0)
GPIO29	BOOT_CONFIG(2)	FASTBOOT_SEL(1)
GPIO108	BOOT_CONFIG(3)	FASTBOOT_SEL(2)
GPIO98	BOOT_CONFIG(4)	FASTBOOT_SEL(3)

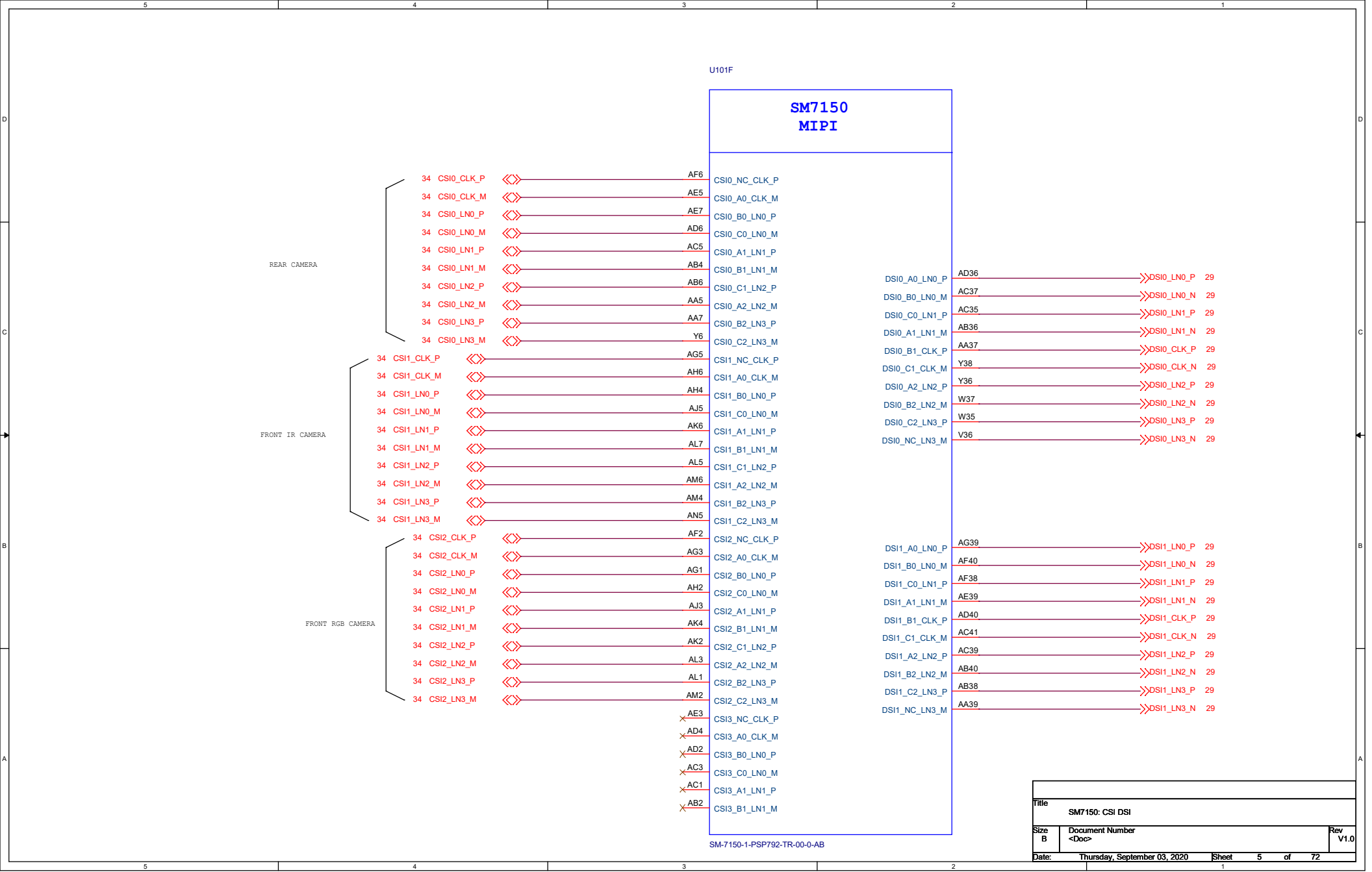
BOOT OPTIONS	BOOT CONFIG BITS			
	4	3	2	1
eMMC->SD->USB3.0->EDL (eDL path- USB only)	0	0	0	0
SD->eMMC->eDL (eDL path USB only)	0	0	0	1
SD->eDL (eDL path- USB only)	0	0	1	0
UFS HS G1->eDL (eDL path- USB only)	0	1	0	0
USB->eDL (eDL Path : SD then USB)	0	0	1	1
UFS 1-LANE PWM G4->EDL (eDL path- SD then USB)	1	0	0	0



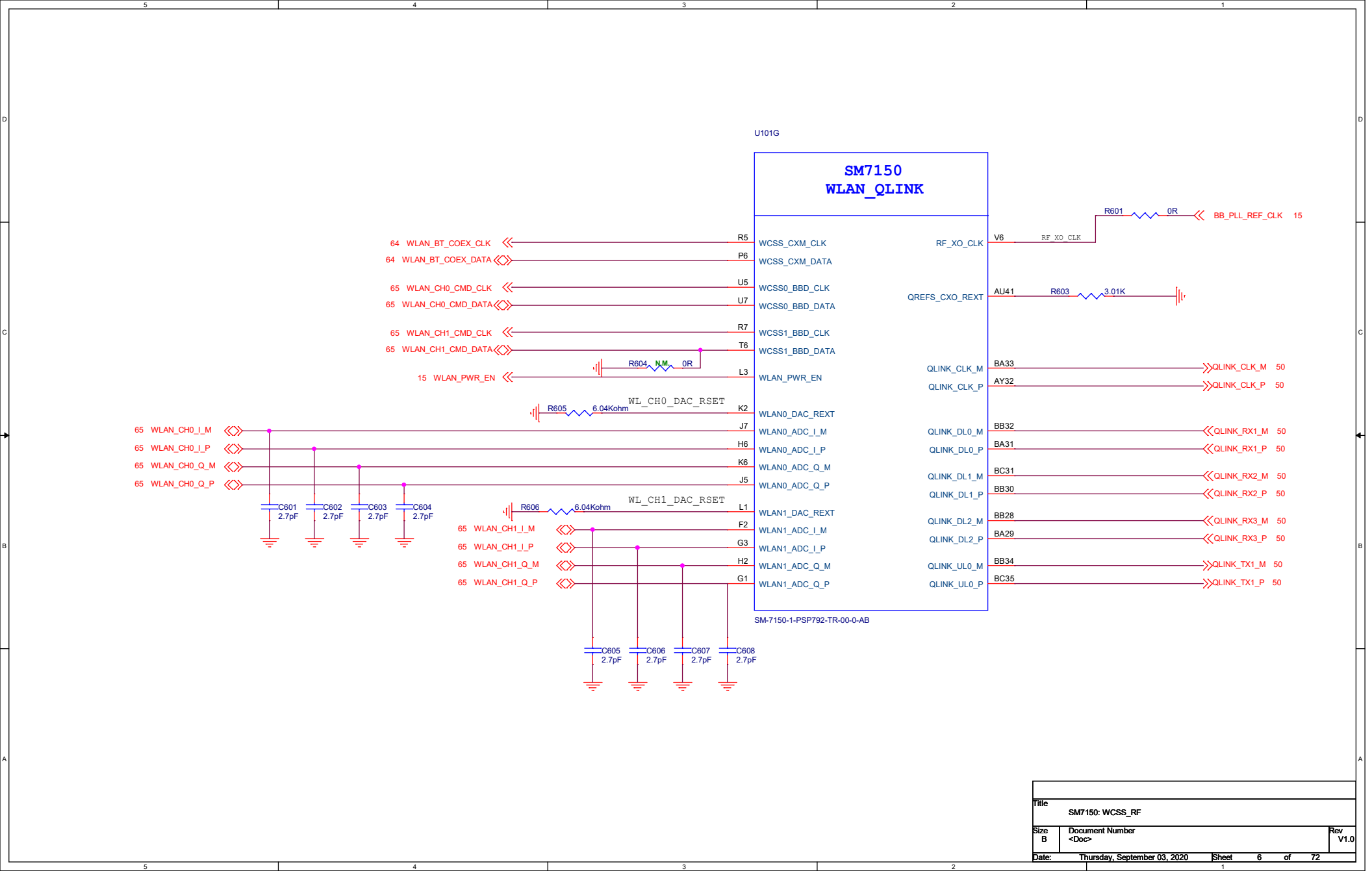
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Size	Document Number	Rev	
C	<Doc>	V1.0	
Date:	Thursday, September 03, 2020	Sheet	2 of 72



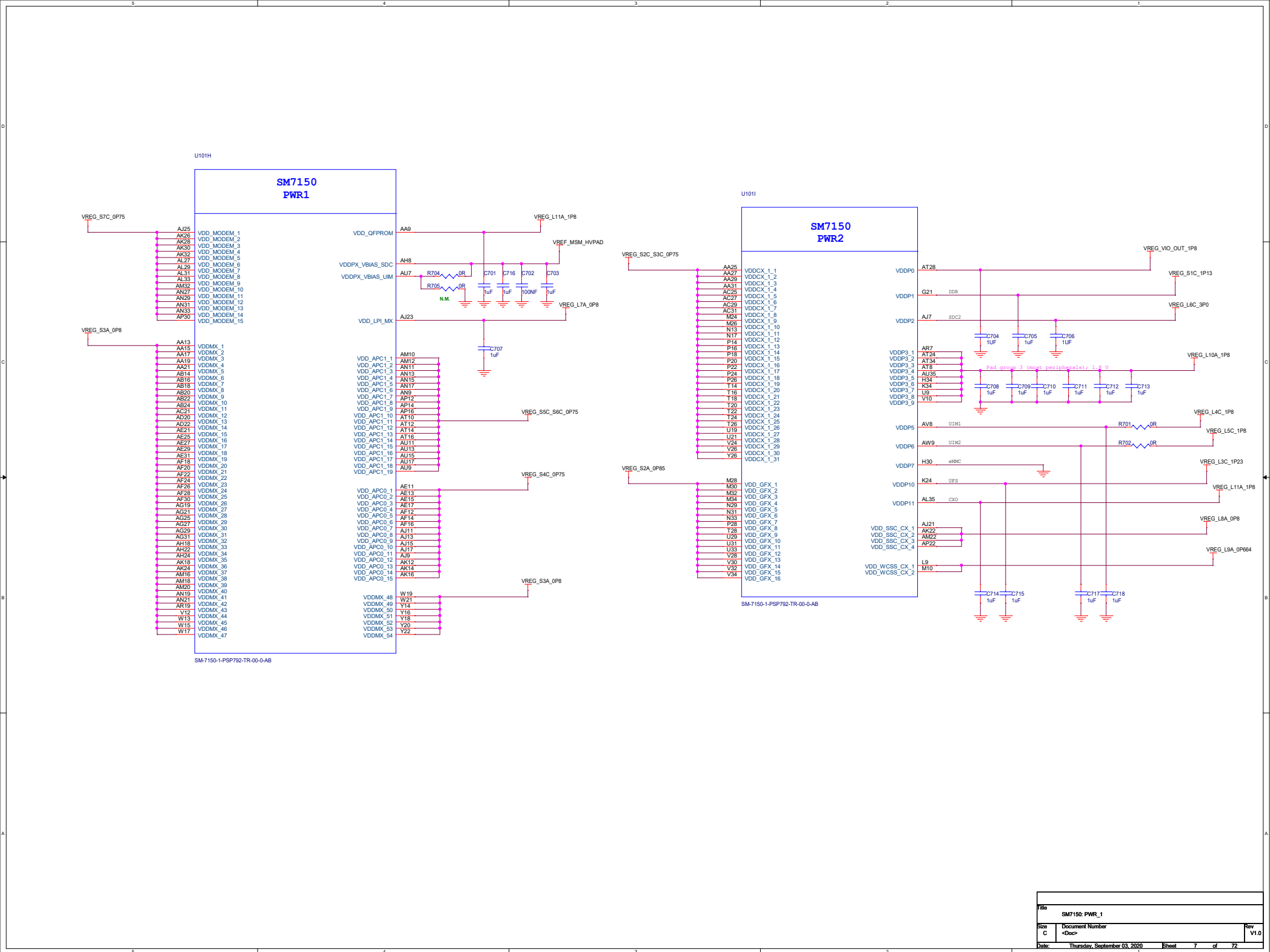


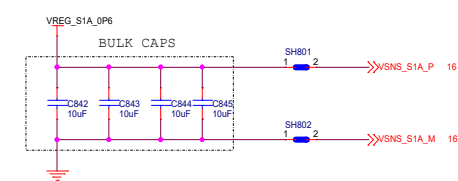
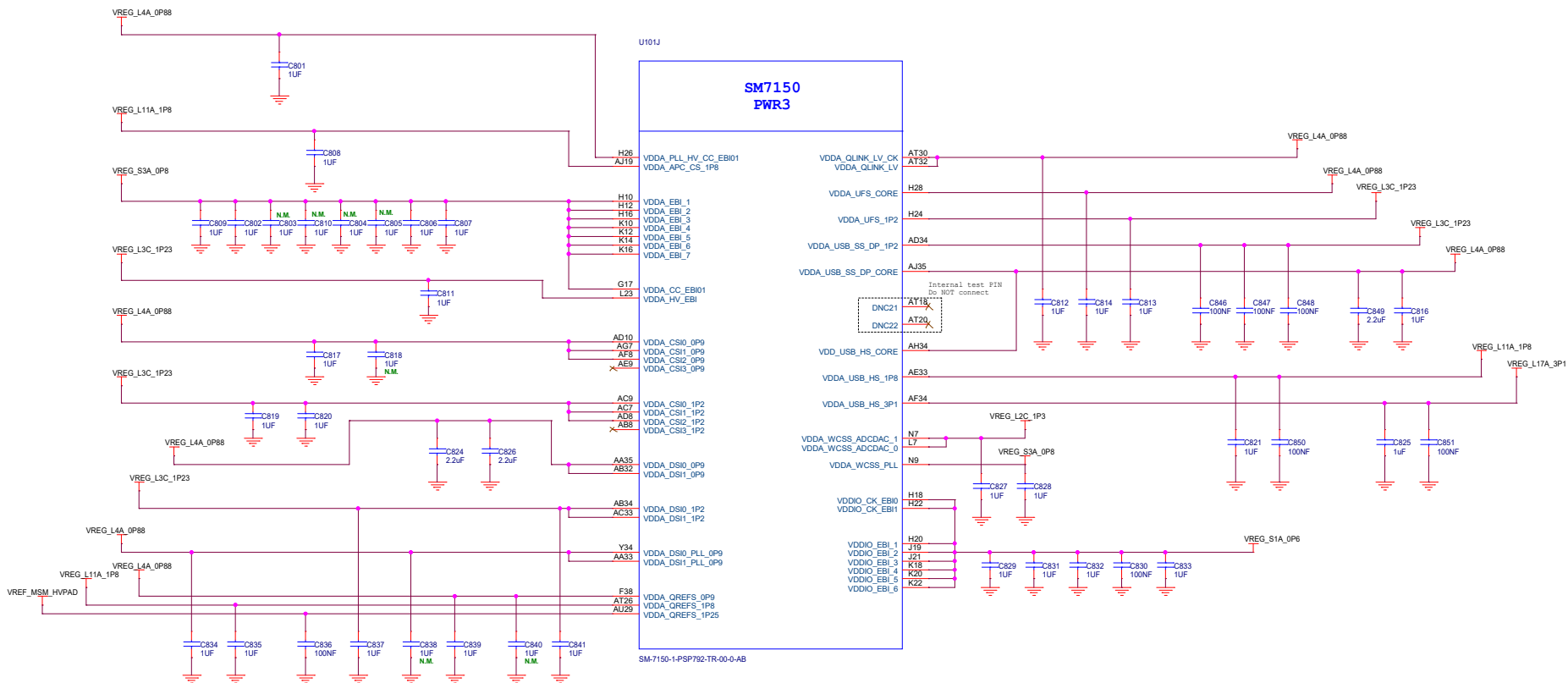


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SM7150: CSI DSI			
Size	Document Number	Rev	
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Date:	Thursday, September 03, 2020	Sheet	5 of 72

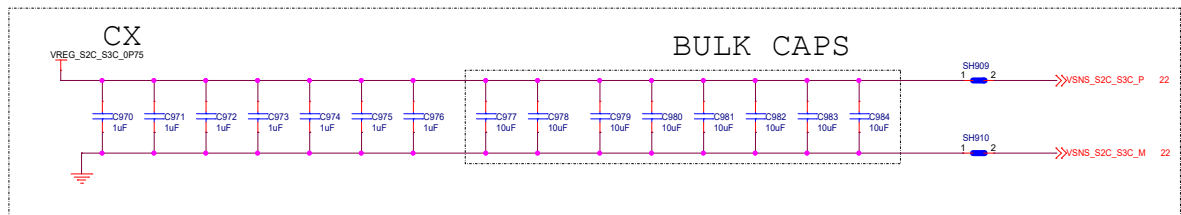
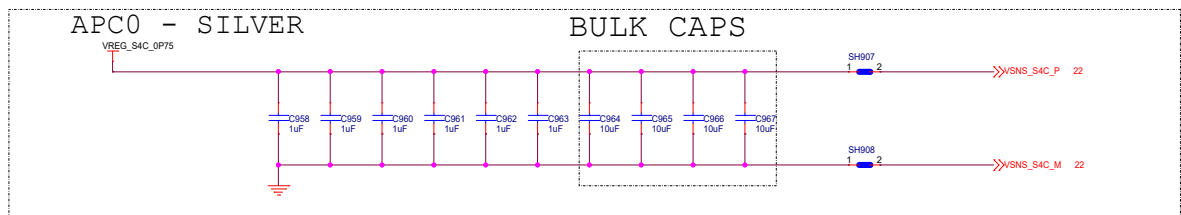
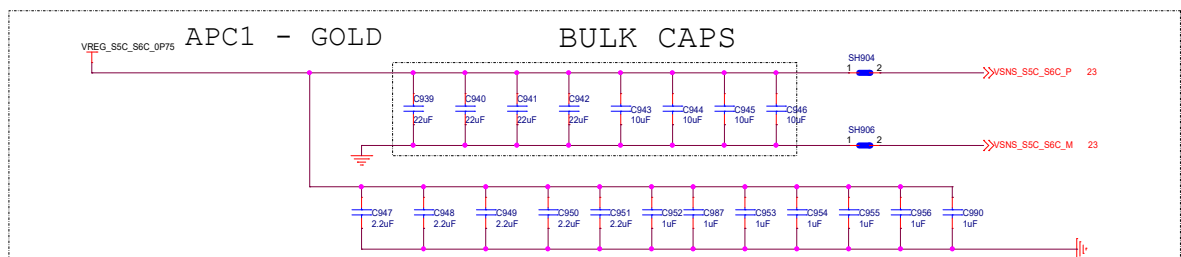
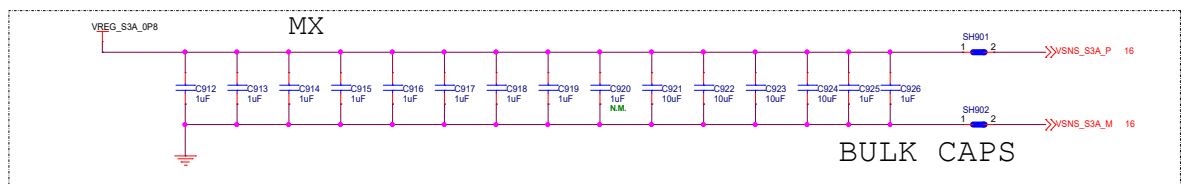
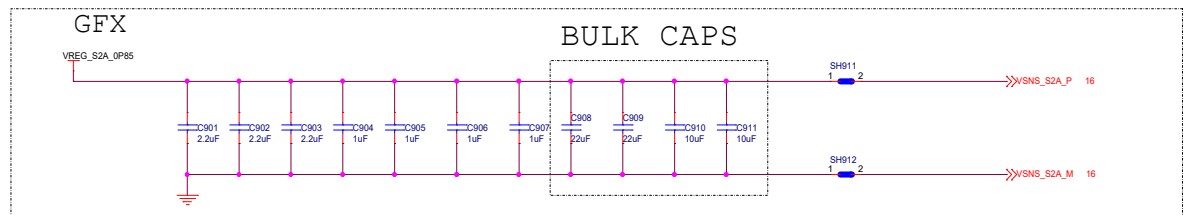


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Size	Document Number	Rev	
B	<Doc>	V1.0	
Date:	Thursday, September 03, 2020	Sheet	6 of 72

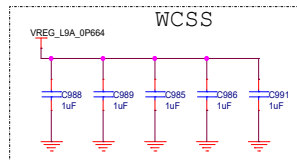
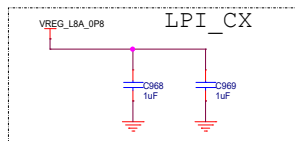
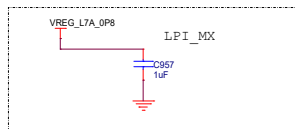
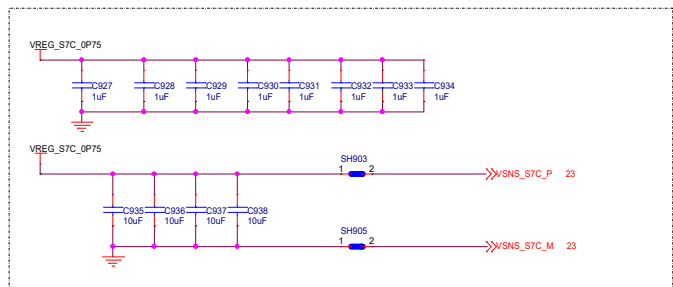




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SM7150: PWR_2			
Size	Document Number	Rev	
C	<Doc>	V1.0	
Date:	Thursday, September 03, 2020	Sheet	8 of 72

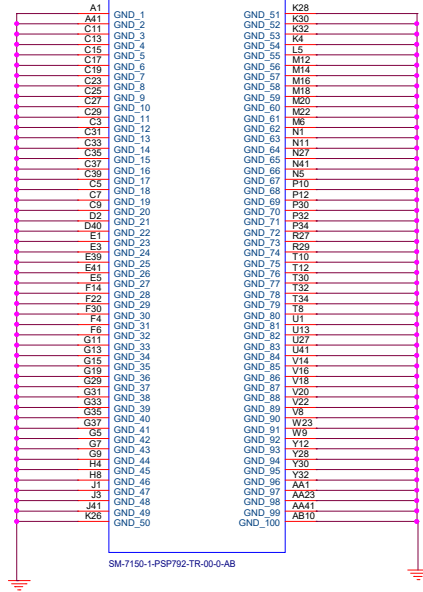


MODEM



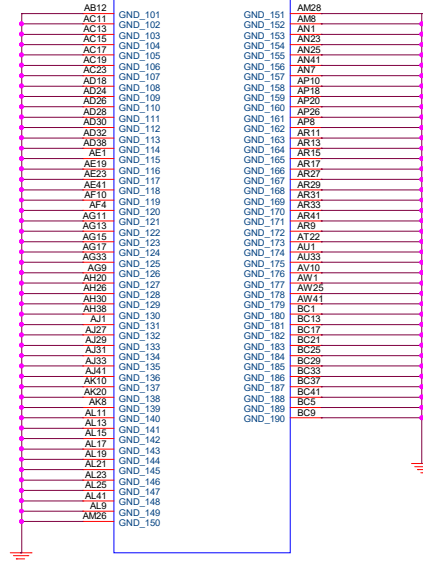
U101K

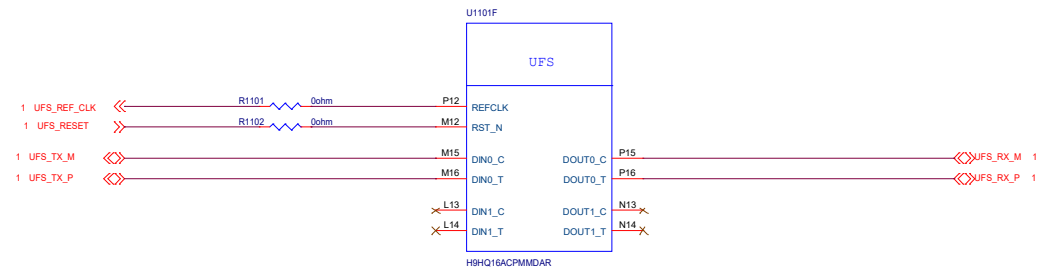
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GND1



U101L

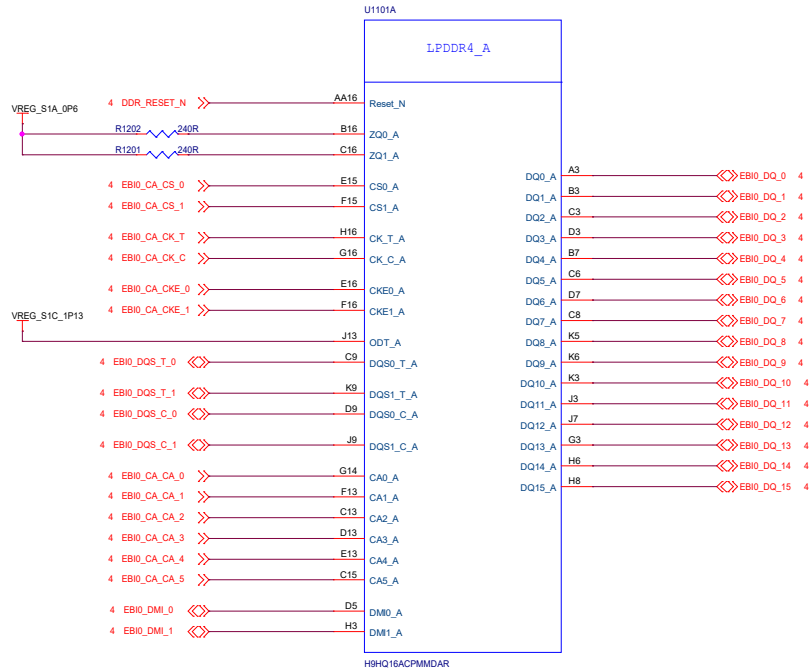
SM7150
GND2



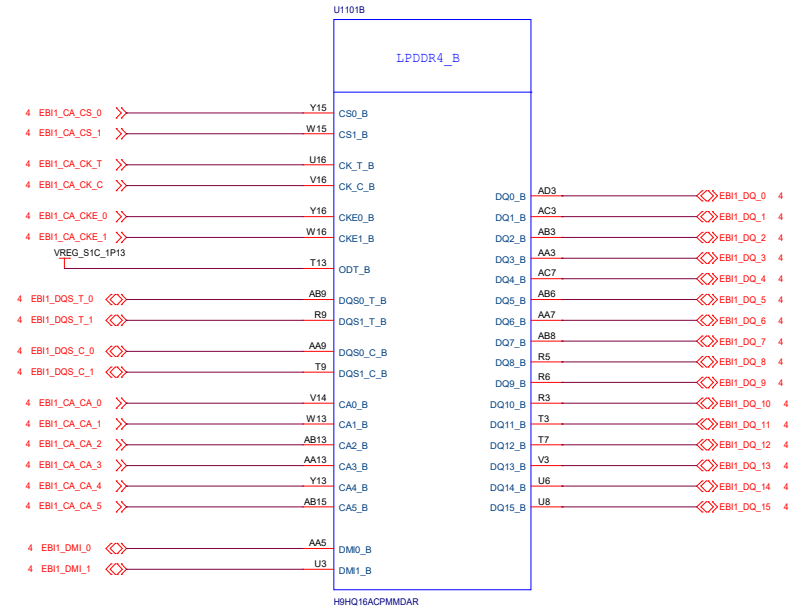


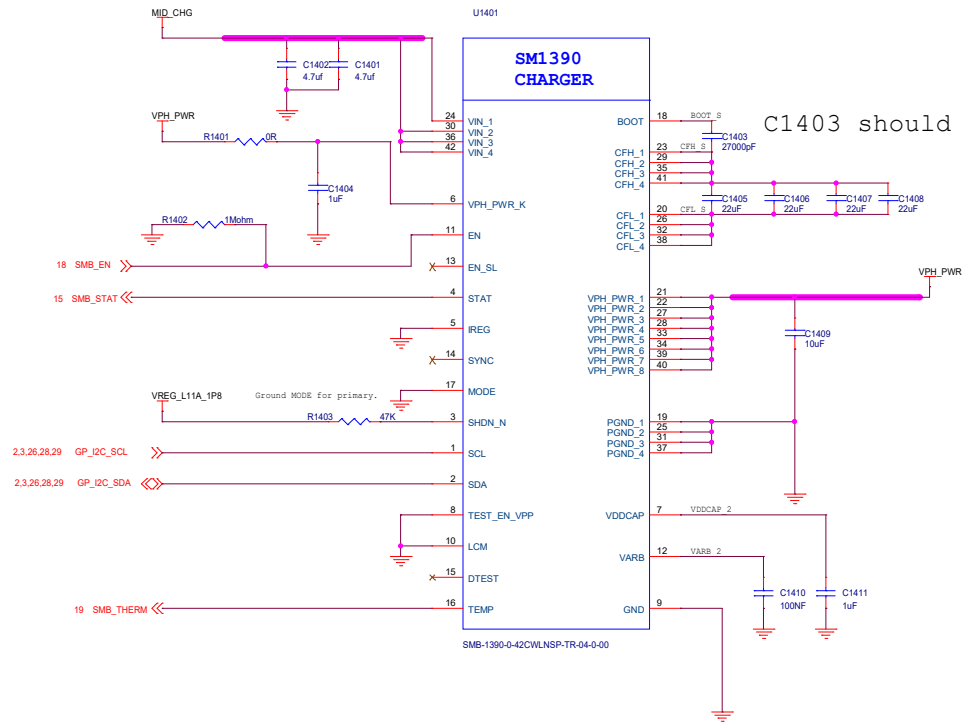
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SM7150- uMCP_UFS		
Size	Document Number	Rev
C	<Doc>	V1.0
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LPDDR4_A



LPDDR4_B

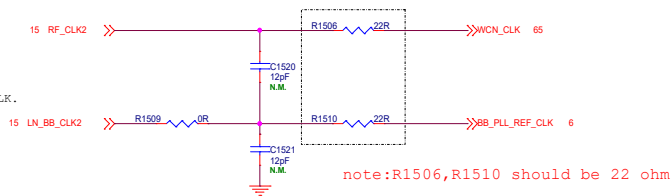
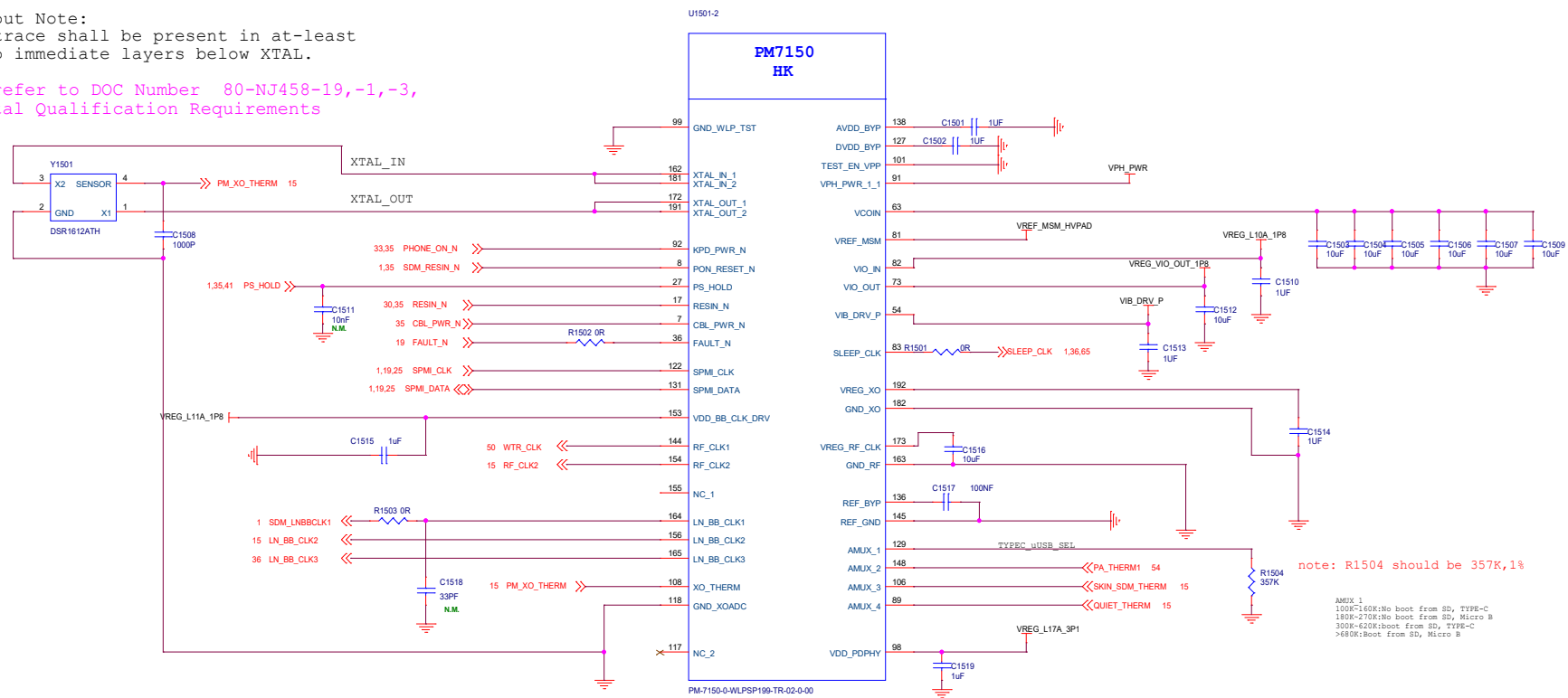




C1403 should be 27nF, >=16v

No trace shall be present in at-least
two immediate layers below XTAL.

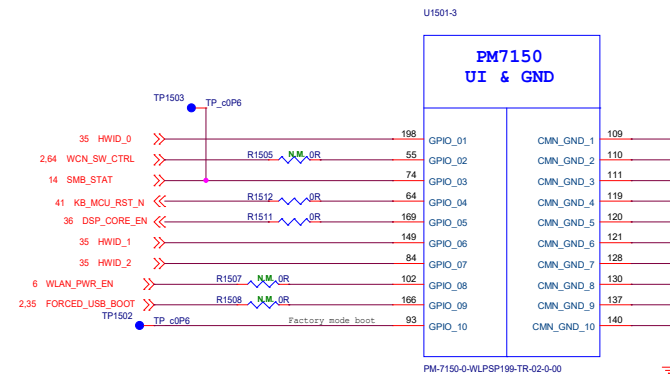
Pls refer to DOC Number 80-NJ458-19,-1,-3,
Crystal Qualification Requirements



```

1. WLAN_5G_CLK_OUT:
R1402, C1419, C1418, R1403, R0905 DNI
2. Divided CLK of RFCLK2(LN_BB_CLK2 DIV):
R1402, R0906, C6802, C6803, R6801 DNI
3. LN_BB_CLK2 (Default)
C1418, C1419, R0906, C6802, C6803, R6801 DNI
POR is option 3

```



Title PM7150: CLK_CONTROL_GND			
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VIN_GR1: VIN_L11_L12_L13
VIN_GR2: VIN_L10_L14_L15
VIN_GR3: VIN_L1
VIN_GR4: VIN_L2_L3
VIN_GR5: VIN_L5_L16_L17_L18_L19
VIN_GR6: VIN_L6
VIN_GR7: VIN_L9
VIN_GR8: VIN_L4_L7_L8

CAD Note:
Local Cap: Trace from pin to Cout must be <5nH and <25mOhm
Capless LDO (cap at load): Trace from pin to load cap must meet PMN requirements

Input Caps to LDO groups are required to meet ESL spec
Place cap before current splits
into GR8 and GR4 for S4A
and into GR6 and GR7 for S3A.
LDO input caps should be placed close to the LDO input pins.

C838 need not be mounted if the LDO input spec
($R_{in_PCB} < 20m\Omega$ and $L_{in_PCB} < 5nH$) can be met..

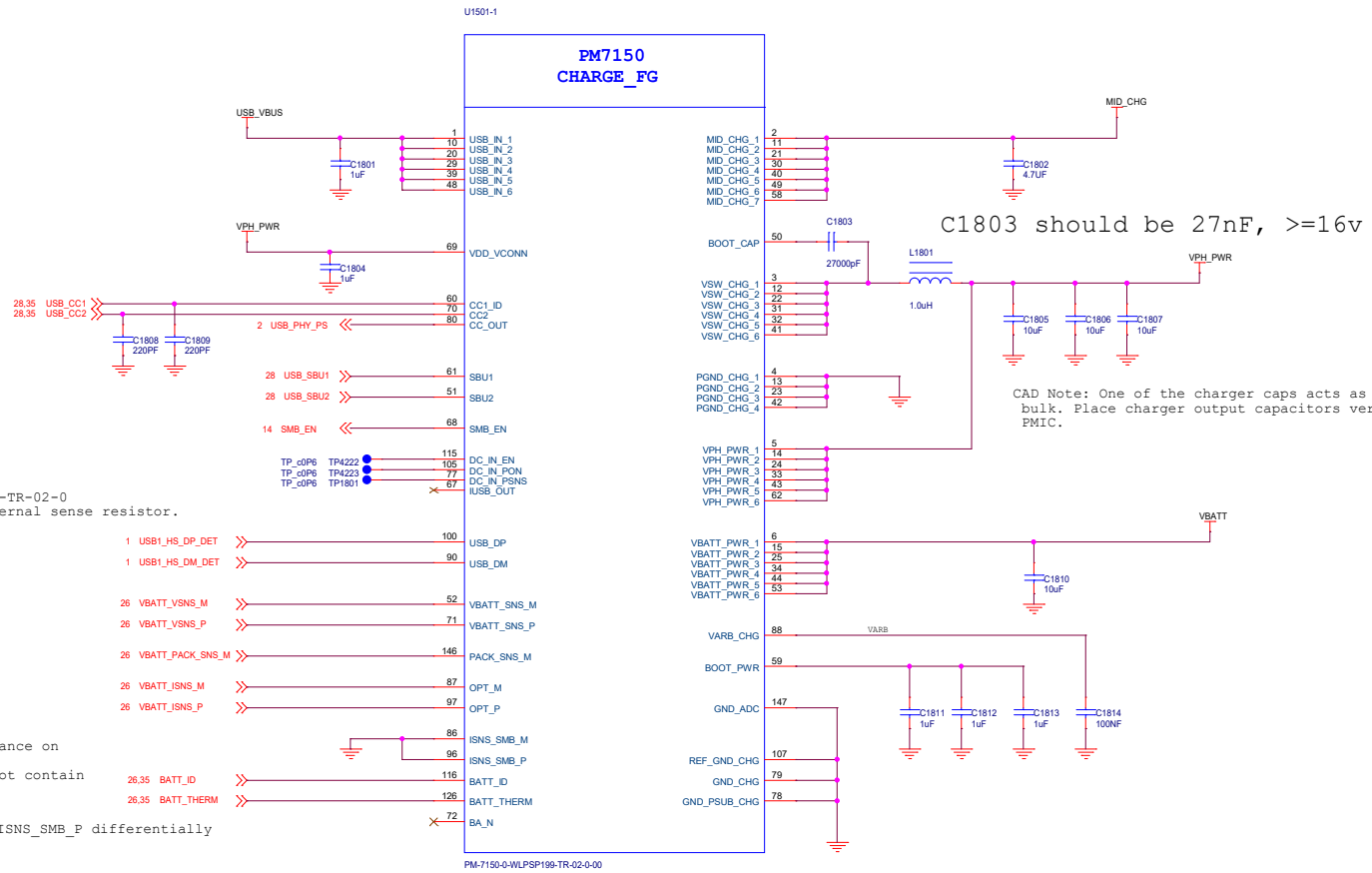
PSEUDO CAPLESS LDOs
For CAPLESS LDOs: If decaps on the load side do not
add up to LDO spec, then install the cap close to the PMIC

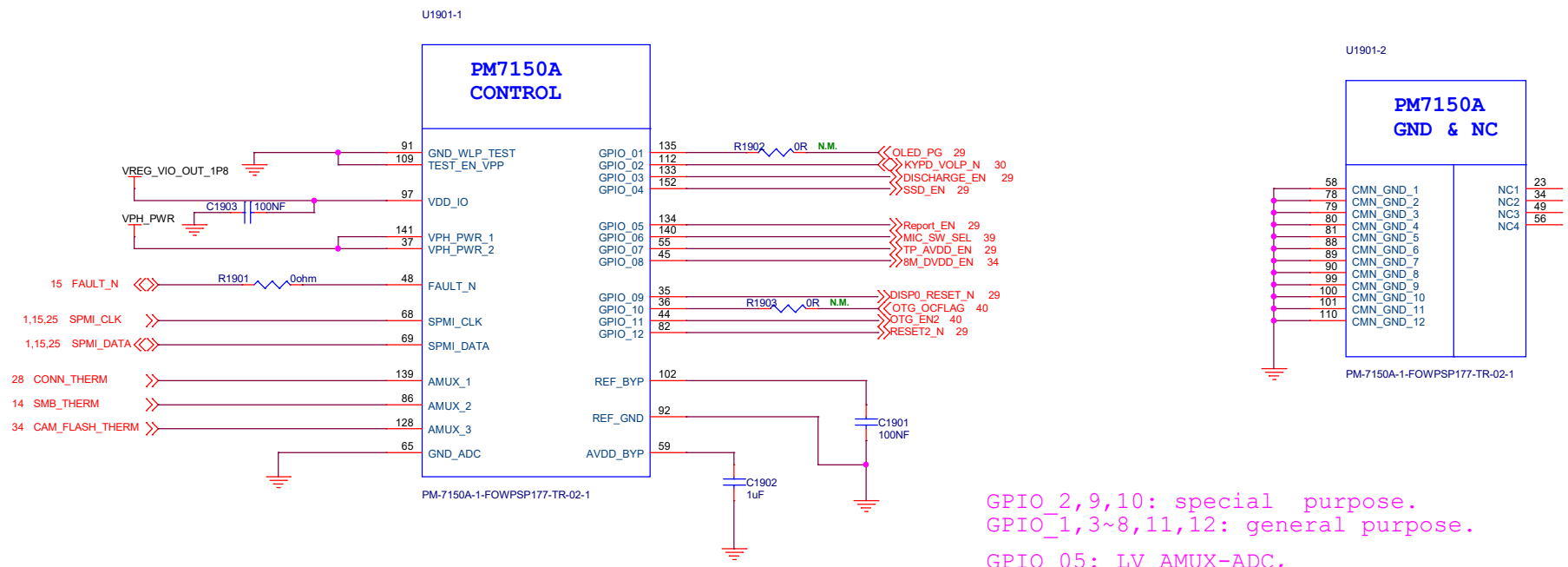
Title			PM7150 LDOs
Size	Document Number	Rev	
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Note: Ensure that PM-7150-1-WLPSP199-TR-02-0 is used for current sensing with external sense resistor.

Note: Do not place any capacitance on BATT_THERM or BATT_ID nets. Ensure battery packs also do not contain any capacitance.

CAD Note: Route ISNS_SMB_M and ISNS_SMB_P differentially



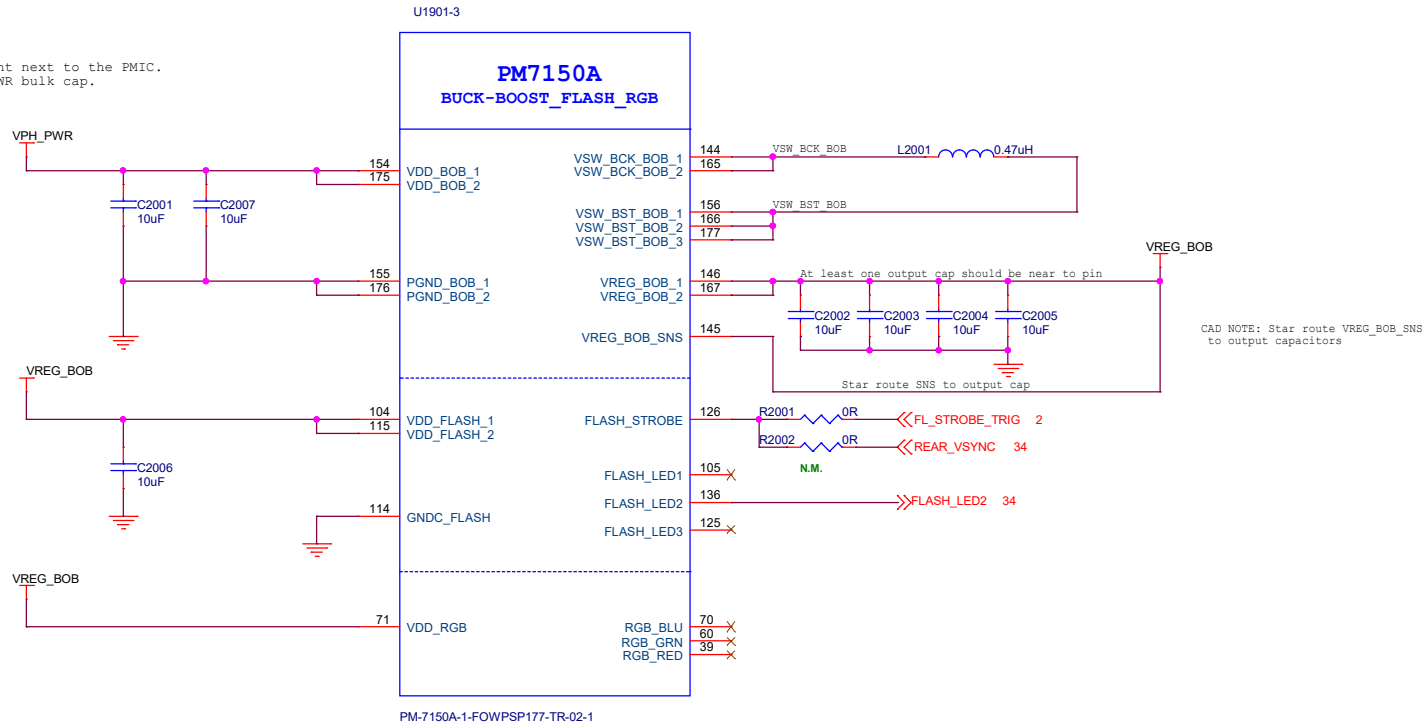


GPIO_2,9,10: special purpose.
GPIO_1,3~8,11,12: general purpose.
GPIO_05: LV AMUX-ADC,
GPIO_06: LV AMUX-ADC,
GPIO_07: MV AMUX-ADC,
GPIO_10: MV AMUX-ADC,

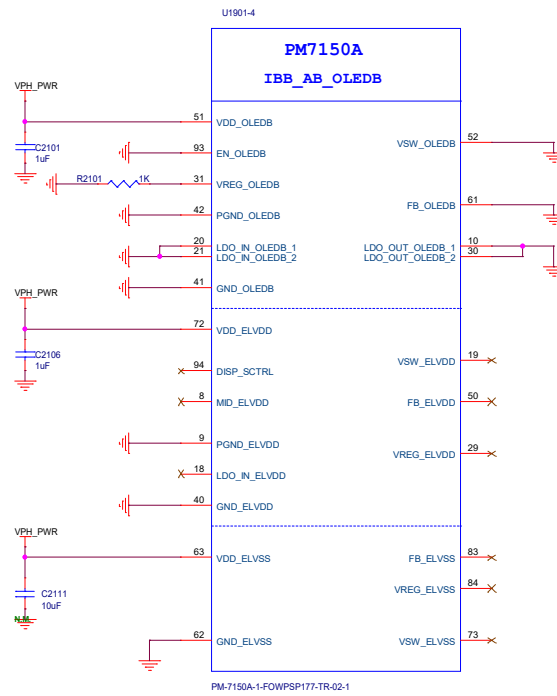
Title			
PM7150A AMOLED			
Size	Document Number	Rev	
B	<Doc>	V1.0	
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CAD Note: Place C33 right next to the PMIC.
This also acts as VPH_PWR bulk cap.

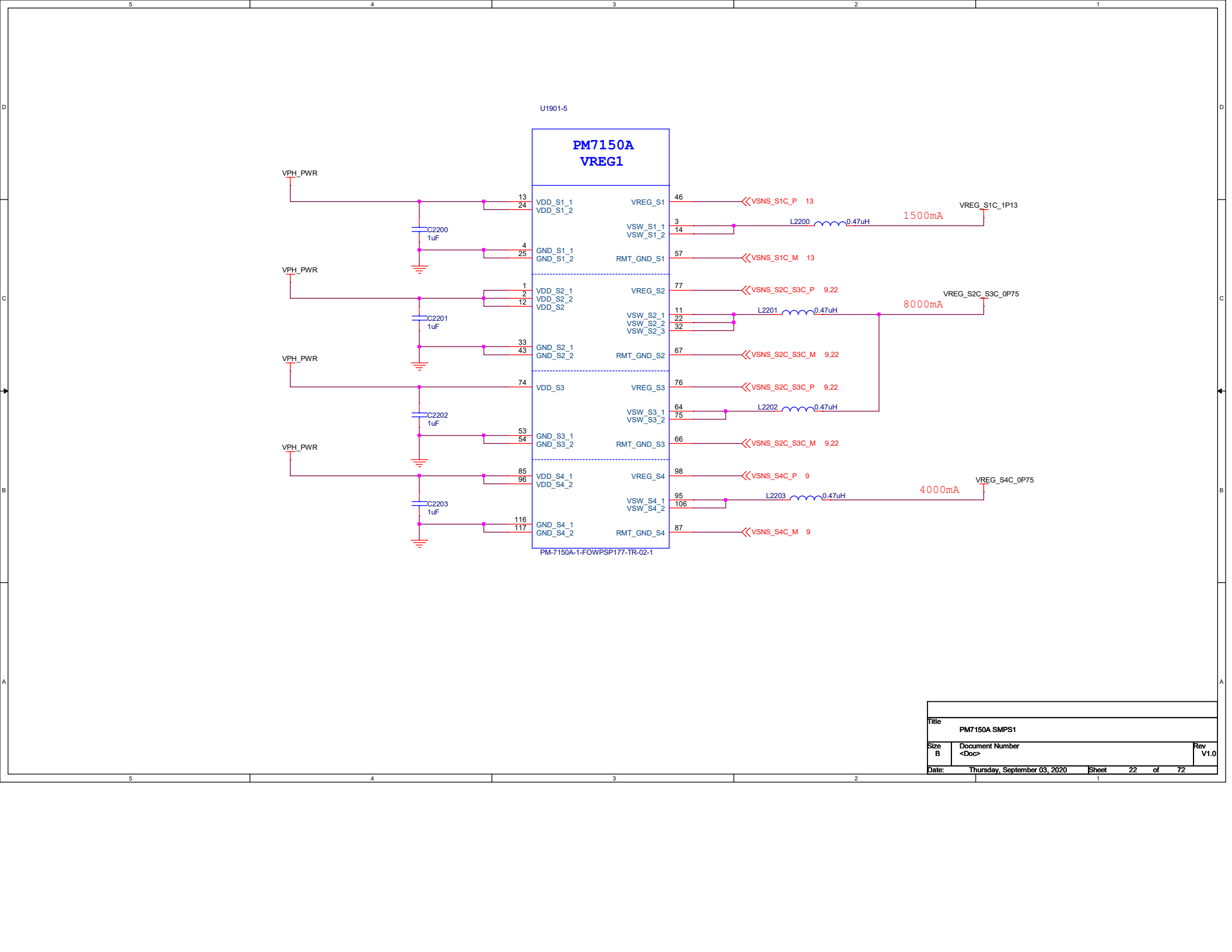
CAD NOTE: Layout Note:PGND_BOB
"Dedicated trace from pin to COUT1 and Cin.
Dedicated vias from cap directly to main gnd plane.
Trace and vias should be able to handle 3A of
continuous current.
Do NOT connect to any other grounds."



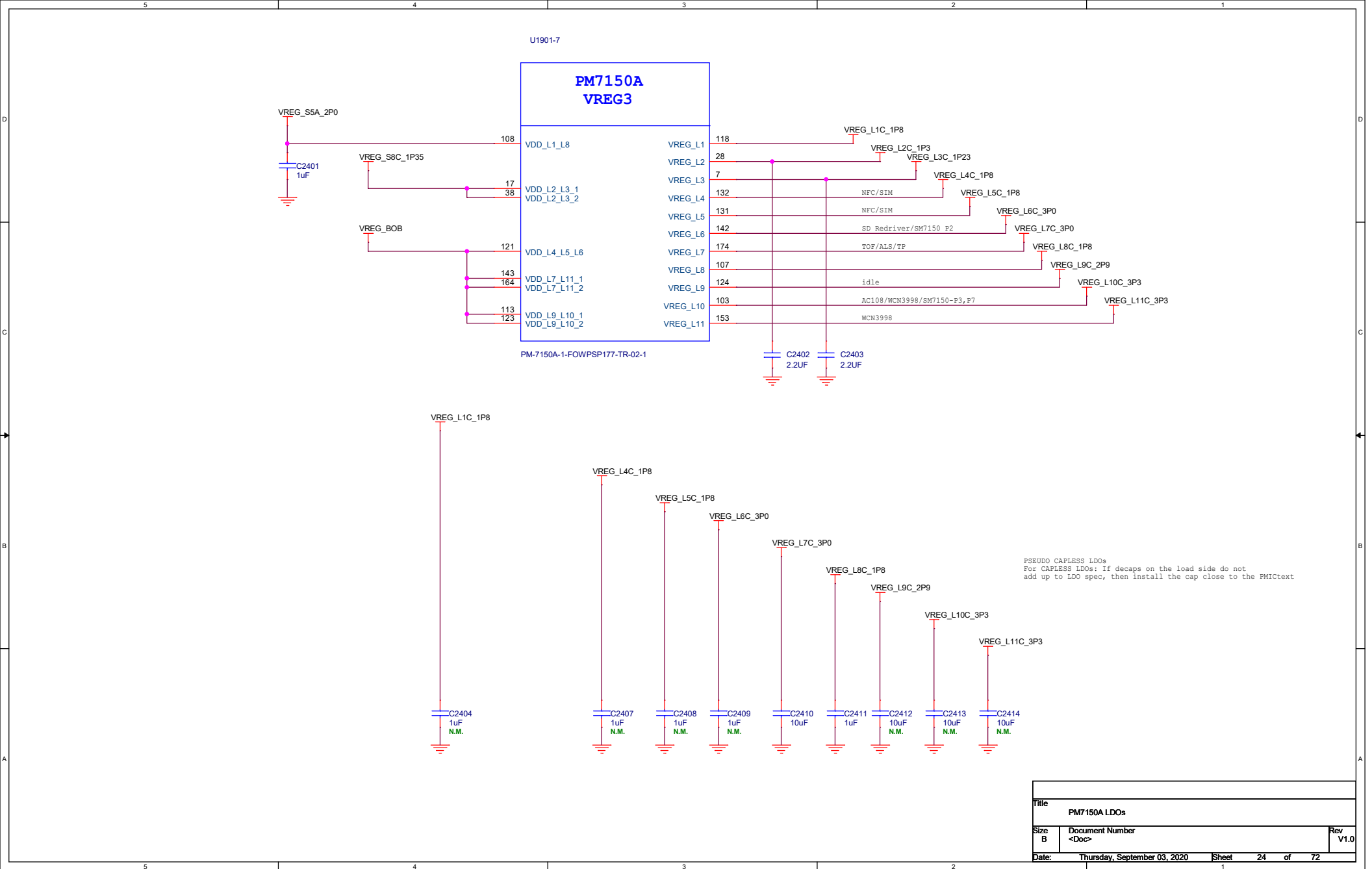
Title		
PM7150A BOB_FLASH_RGB		
Size	Document Number	Rev
B	<Doc>	V1.0
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File		
PM7150 OLED		
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C	<Doc>	V1.0
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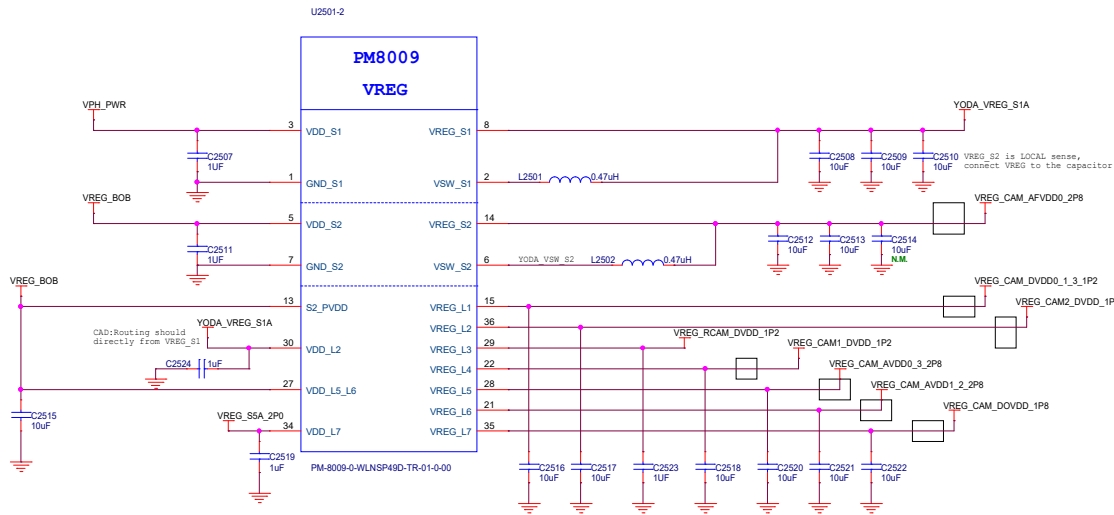
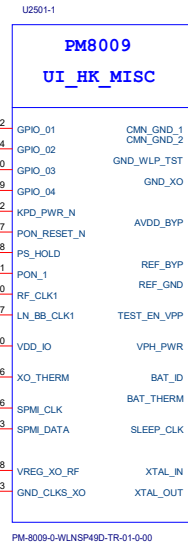
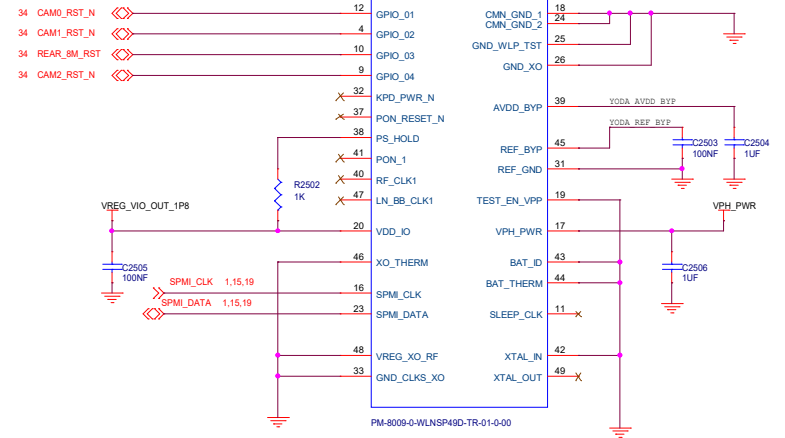
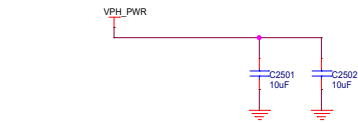


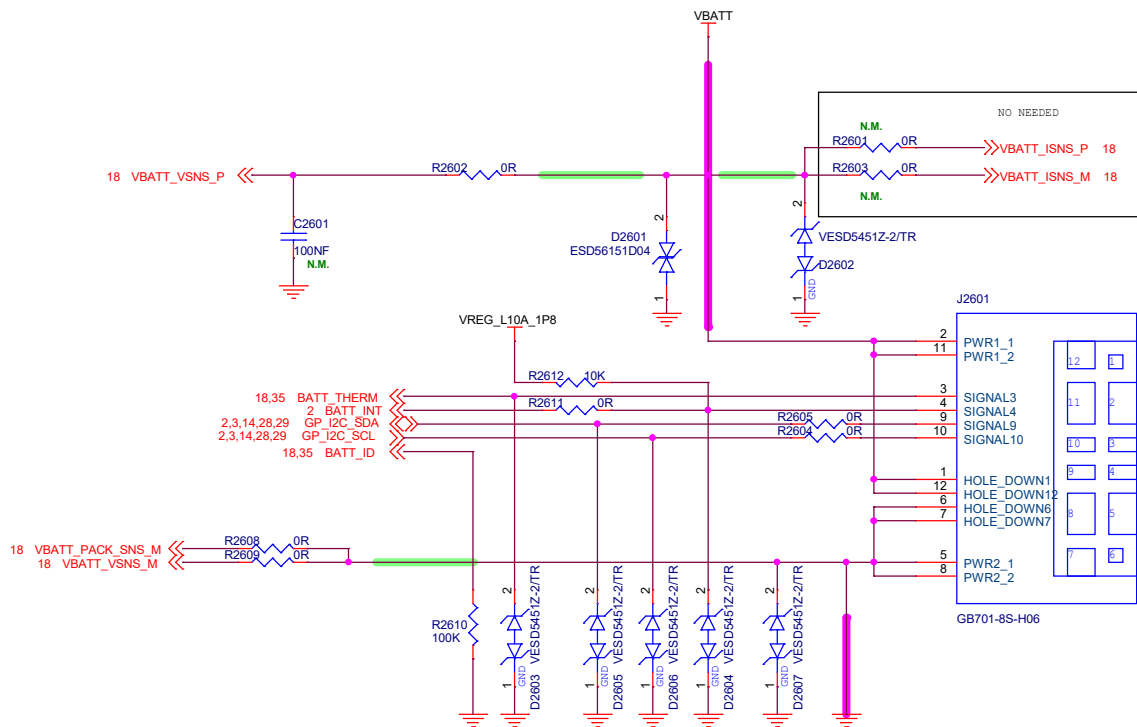
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PM7150A SMPS1		
Size B	Document Number <Doc>	Rev V1.0
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Title		
PM7150A LDOs		
Size	Document Number	Rev
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Critical Layout Guidelines for VREG_XO (Check Layout Checklist)
Preferred: Short, dedicated route to VREG_XO cap,
away from noisy signals and dedicated via to main ground plane at cap.
Acceptable: Dedicated via directly to main ground plane at the GND_CLKS_XO pin
and at VREG_XO cap (without routing to cap)
Do NOT connect to any other ground.
Loop DCR must be <1000 mohm
Loop inductance must be <3 nH.

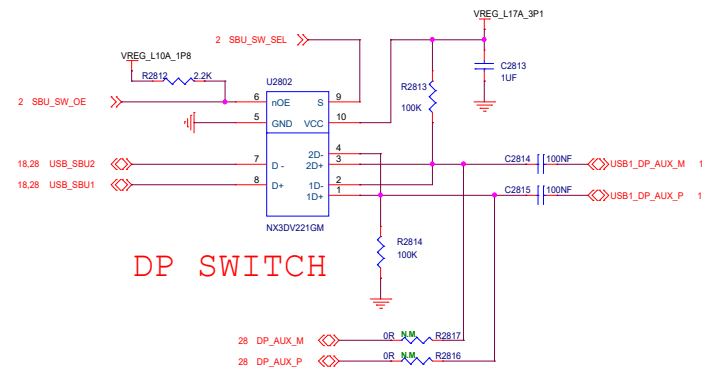
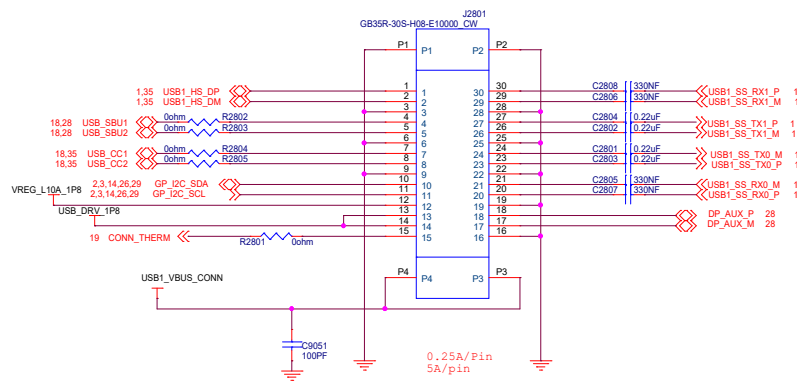
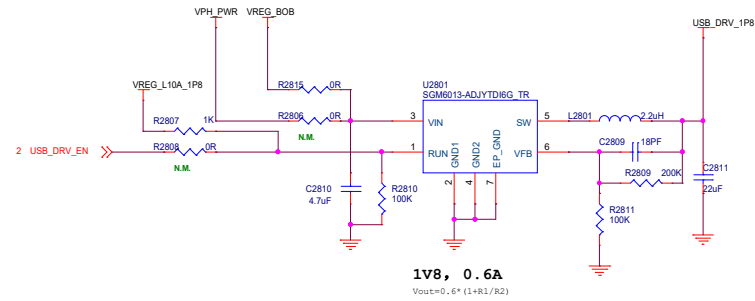


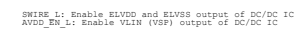


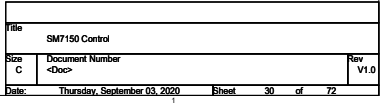
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SM7150 Control		
Size	Document Number	Rev
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Date:	Thursday, September 03, 2020	Sheet 26 of 72

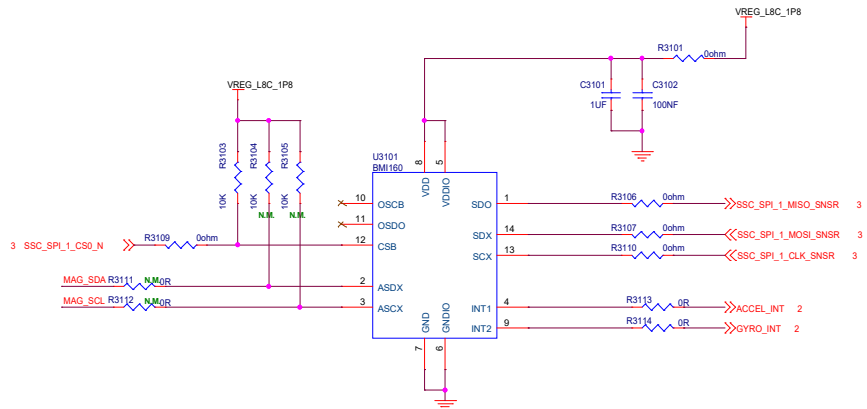


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Size	Document Number	Rev
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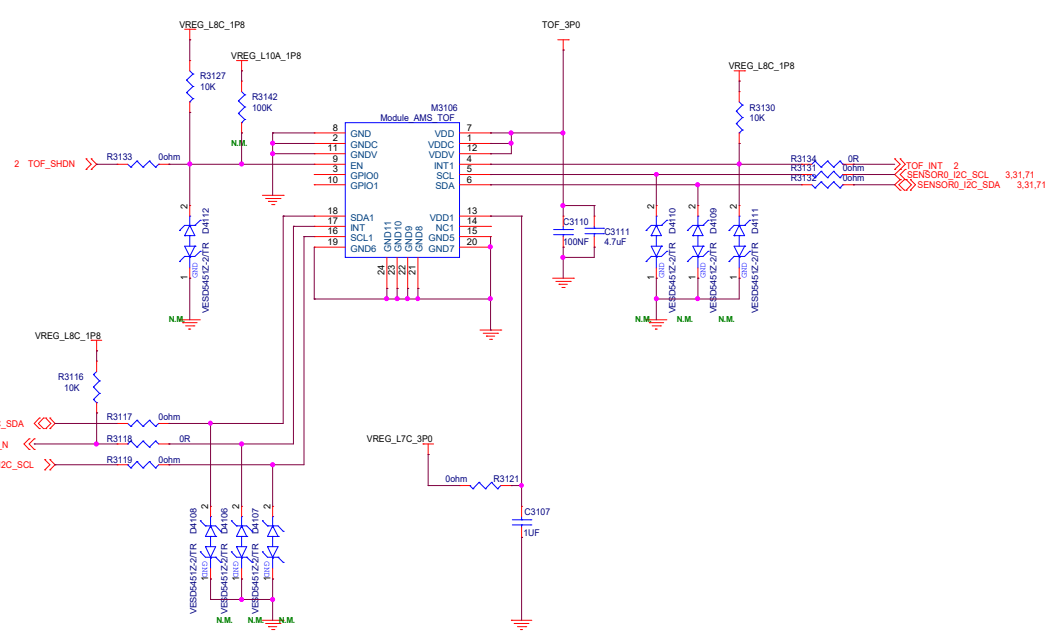
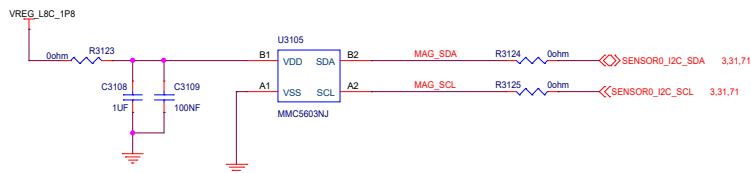
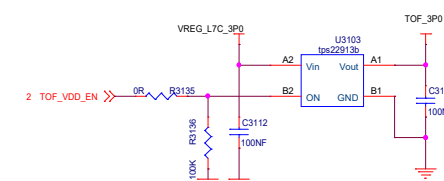
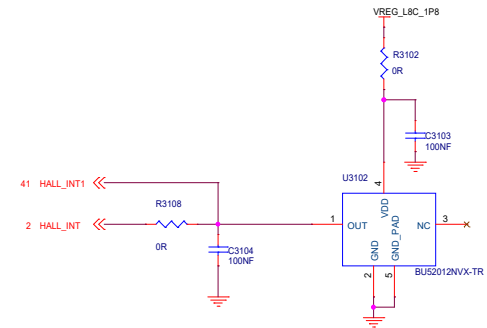


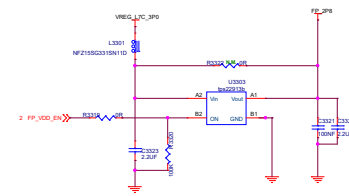
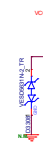
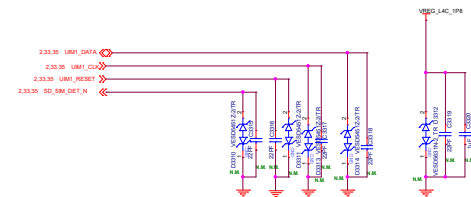
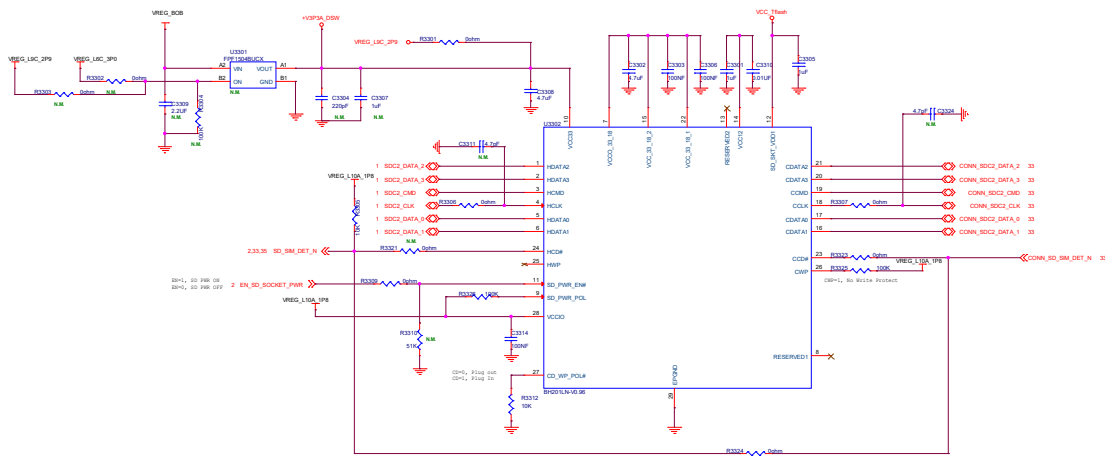




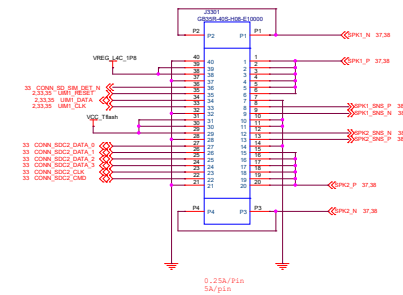
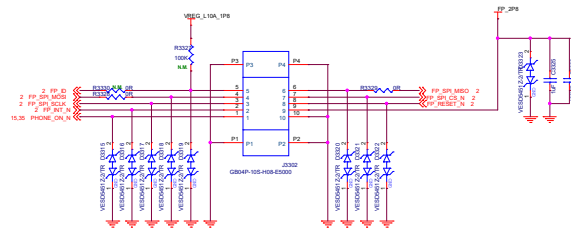


P2P with ST LSM6DS3TR-C,
 LSM6DS3TR-C: install Rpu in Pin 2,3
 BMI160: NM Rpu in Pin 2,3

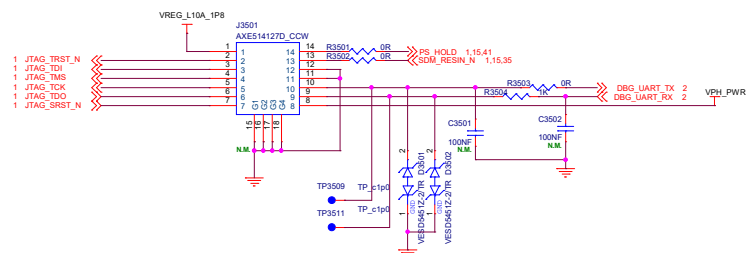




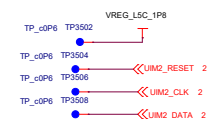
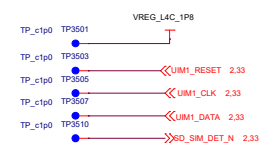
20191105:
Change 34 pin connector to 48pin;



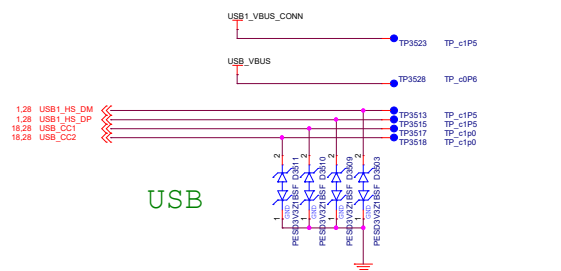
Doc	SM100-SM-BD
Rev	Document Number
Rev	Docu
Docu	Docu



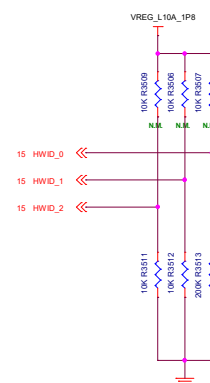
JTAG FPC CONNECTOR (PHINNY)



Factory SIM Test Point

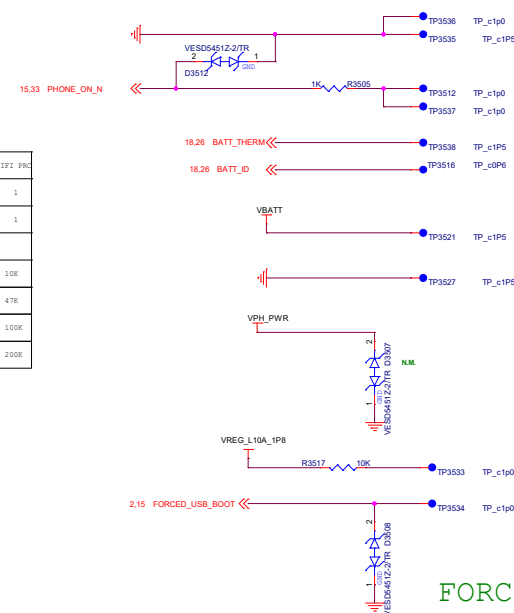


USB



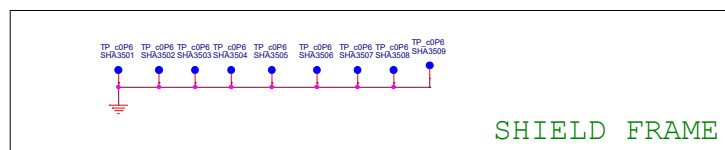
HW-ID

	LTE ROW	LTE FRC	NFI ROW	NFI
HWID_1	0	0	1	1
HWID_2	0	1	0	1
HWID_0_EVB	OR	OR		
HWID_0_EVT	10K 0.17V	10K	10K	10K
HWID_0_EVT1	47K 0.6V	47K	47K	47K
HWID_0_EVT2	100K 0.938V	100K	100K	100
	200K	200K	200K	200

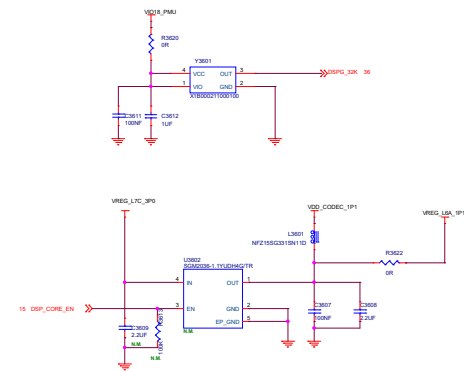


VBAT

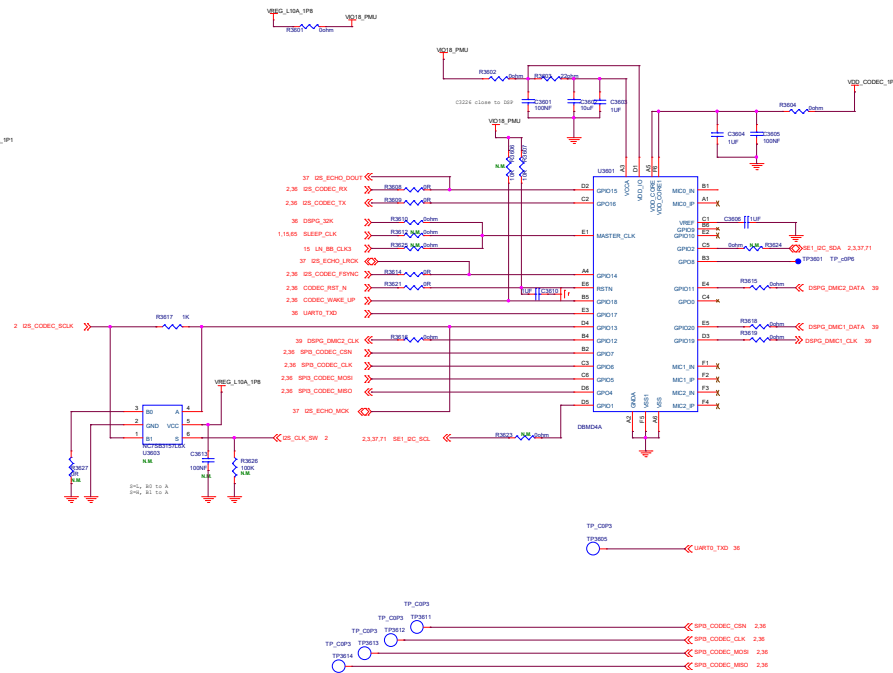
FORCE BOOT



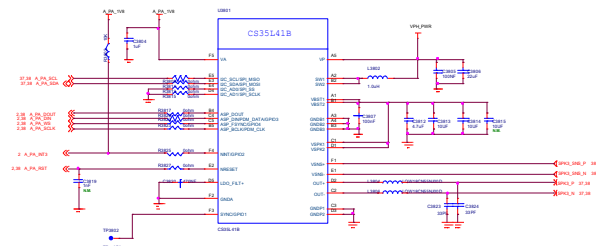
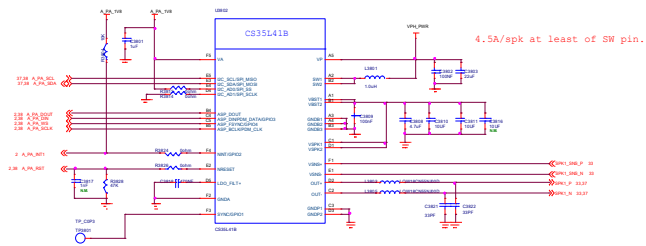
SHIELD FRAME



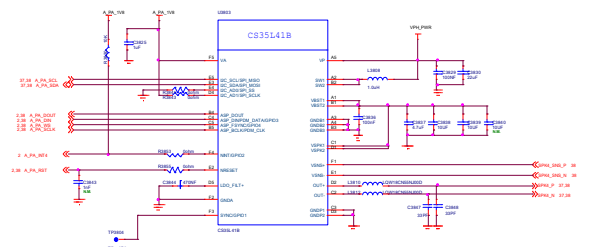
SGM2036 VIN>2.5V

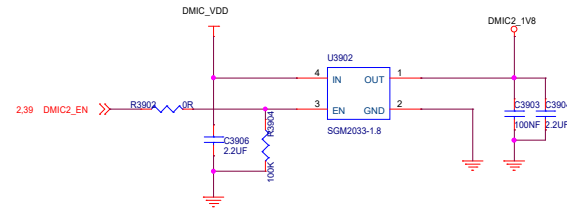
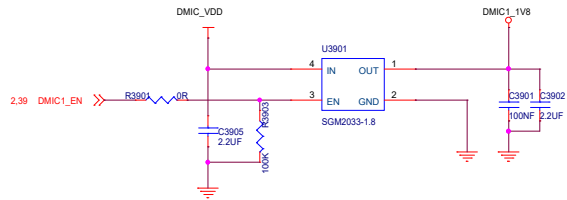


T2C ADDRESS=0x35

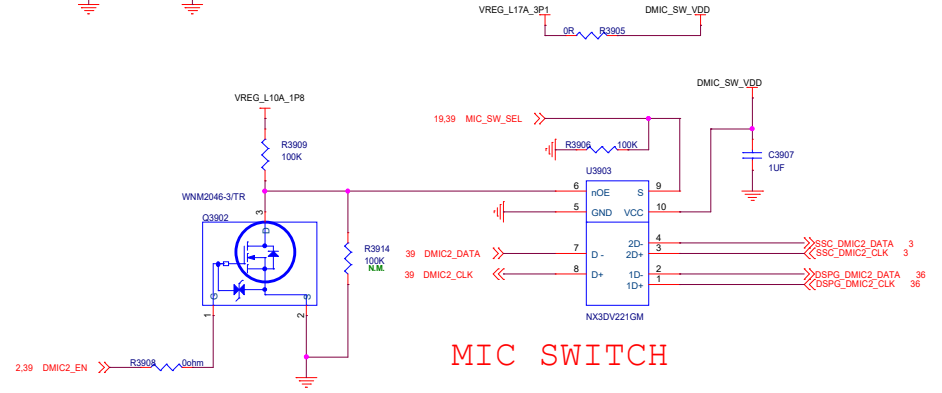
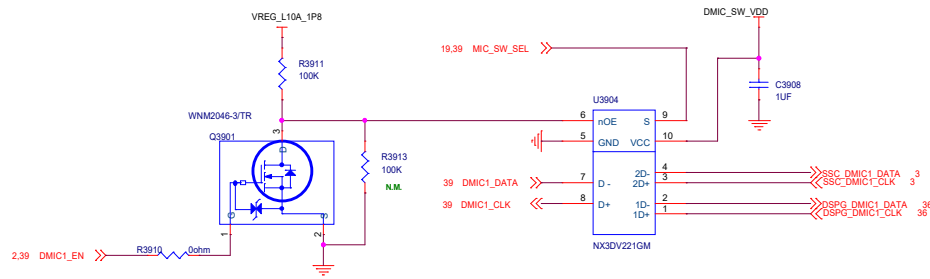
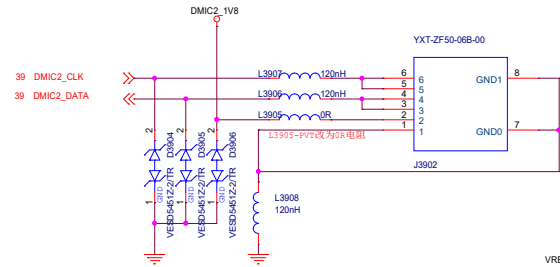
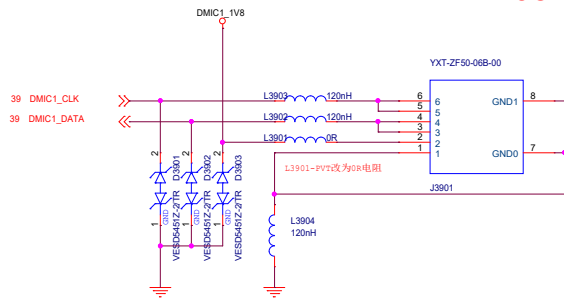


The schematic diagram illustrates the internal circuitry of the CS35L41B audio amplifier. Key components include the CS35L41B IC, a 1.5V regulator, a 1.5V regulator, a 1.5V regulator, and a 1.5V regulator. The circuit is powered by a 1.5V regulator and a 1.5V regulator. The output is connected to a 1.5V regulator and a 1.5V regulator. The circuit is designed for a 1.5V regulator and a 1.5V regulator.



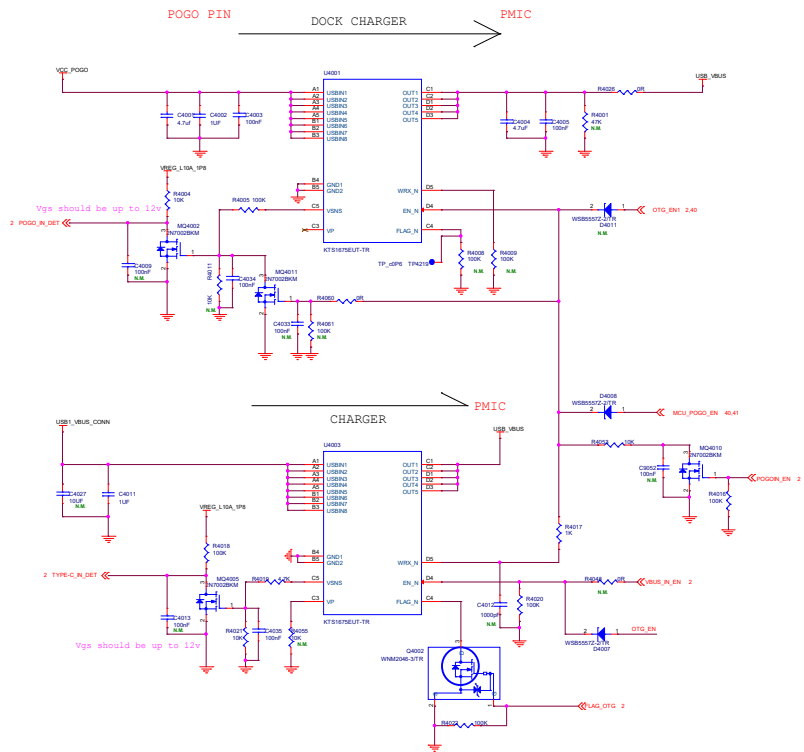
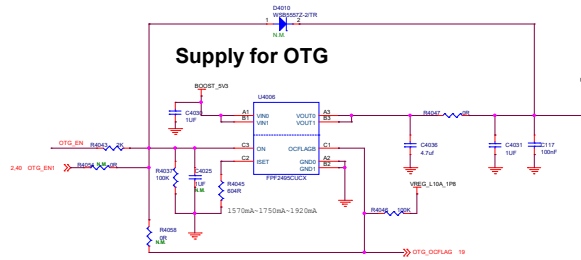


SGM2033: VIN= (VOUT+1V) to 5.5V



MIC SWITCH

S OE PATH
L L D=1D+
H L D=2D+
X H switch off





SM7150 Power Sequencing

1. VDDMX (on-chip memory), VDDA_EBI (EBI PHY circuits),VDDA_CC_EBI01, and VDDA_WCSS_PLL (WCSS PLL circuits),
2. VDD_LPI_MX (LPI memory),
3. VDDC_X (digital core circuits),
4. VDD_SSC_CX (LPI core),
5. VDDP3 (GEN 1.8 V IO), VDD1 (LPDDR4X VDD1 supply),
6. VDD_WCSS_CX (WCSS core supply),
7. VDDP_X_VBIAS_SDC, VDDP_X_VBIAS_UIM, and VDDA_QREFS_1P25,
8. VDDP1 and VDD2 (LPDDR4X VDD2 supply),
9. VDDIO_EBI (EBI IO supply), VDDIO_CK_EBI0, VDDIO_CK_EBI1 (EBI clock supply),VDDQ (LPDDR4X VDDQ supply),
10. VCCQ2 (UFS/eMMC VCCQ supply),
11. VDDP10 (UFS), VDDA_CSIX_1P2 (MIPI CSI 1.2 V), VDDA_DSIX_1P2 (MIPI DSI 1.2 V),
VDDA_UFS_1P2 (UFS cIock), VDDA_USB_SS_DP_1P2 (USB SS 1.2 V), VDDA_HV_EBI(EBI PHY),
12. VDDA_QREFS_0P9 (QLink reference), VDDA_DSIX_0P9 (DSI core), VDDA_DSIX_PLL_0P9 (DSI PLL),
VDDA_QLINK_LV_CK (QLink clock), VDDA_QLINK_LV (QLink core), VDDA_UFS_CORE (UFS core),
VDDA_CSIX_0P9 (CSI core), VDDA_PLL_HV_CC_EBI01 (EBI PLL), VDD_USB_HS_CORE (USB digital core), VDDA_USB_SS_DP_CORE (USB SS DP core),
13. VDD_QFPROM (QFPROM), VDDP11 (Digital IO), VDDA_USB_HS_1P8 (USB HS1), VDDA_APC_CS_1P8 (APC current sense), VDDA_QREFS_1P8 (QREFS),
14. VDDA_USB_HS_3P1 (USB HS)
15. VDDP2 (SDC2)
16. VDD_MODEM
17. VDD_APC0

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The default power-on sequence across both PMICs (PM7150 and PM7150A) is listed in order here.

sequence.	device:	name:	vout	note
1.	PM7150:	VIO_OUT:	1.8V	PX0 PMIC I/O pads
2.	PM7150A/L:	VREG_BOB:	3.312V	BOB
3.	PM7150A/L:	VREG_S8C:	1.352V	MV sub regulation
4.	PM7150:	VREG_S4A:	1.056V	LV sub regulation
5.	PM7150:	VREG_S5A:	2.04V	HV sub regulation, LDO XO RF
6.	PM7150:	VREG_L3A:	1V	WTR 1 V digital, PON req
7.	PM7150:	VREG_S3A:	0.8V	VDDMX, VDDA EBI PHY, WCSS (CX regulated by L9A)
8.	PM7150:	VREG_L7A:	0.8V	LPI MX
9.	PM7150:	VREG_S2C_S3C:	0.752V	VDDCX including NPU
10.	PM7150:	VREG_L8A:	0.752V	SSC_CX
11.	PM7150:	VREG_L10A:	1.8V	LP4X VDD1, GEN 1.8 V I/O, RFFE 1p8
12.	PM7150:	VREG_L9A:	0.664V	WCSS_CX
13.	PM7150:	VREF_MSM:	1.25V	QREF_PMIC, UIM_BIAS, and SDC Bias
14.	PM7150A/L:	VREG_S1C:	1.128V	VDDPX1 and LP4X VDD2
15.	PM7150:	VREG_S1A:	0.6V	LP4X VDDQ and VDDIO_EBI
16.	PM7150:	VREG_L12A:	1.8V	eMMC/UFS 1.8 V
17.	PM7150A/L:	VREG_L3C:	1.2V	PHY 1.2 V - UFS VCCQ
18.	PM7150:	VREG_L4A:	0.88V	PHY 0.88 V
19.	PM7150:	VREG_L11A:	1.8V	PLL - BBCLK - PHY: USB - UFS
20.	PM7150:	VREG_L17A:	3.088V	PDPHY USB3p1 DP Switch
21.	PM7150A/L:	VREG_L19A:	2.96V	eMMC/UFS VCC
22.	PM7150A/L:	VREG_L6C:	2.96V	SDCard I/O PX2
23.	PM7150A/L:	VREG_L9C:	2.96V	SD/MMC card
24.	PM7150A/L:	VREG_S7C:	0.752V	Modem SS and Q6
25.	PM7150A/L:	VREG_S4C:	0.752V	APC0

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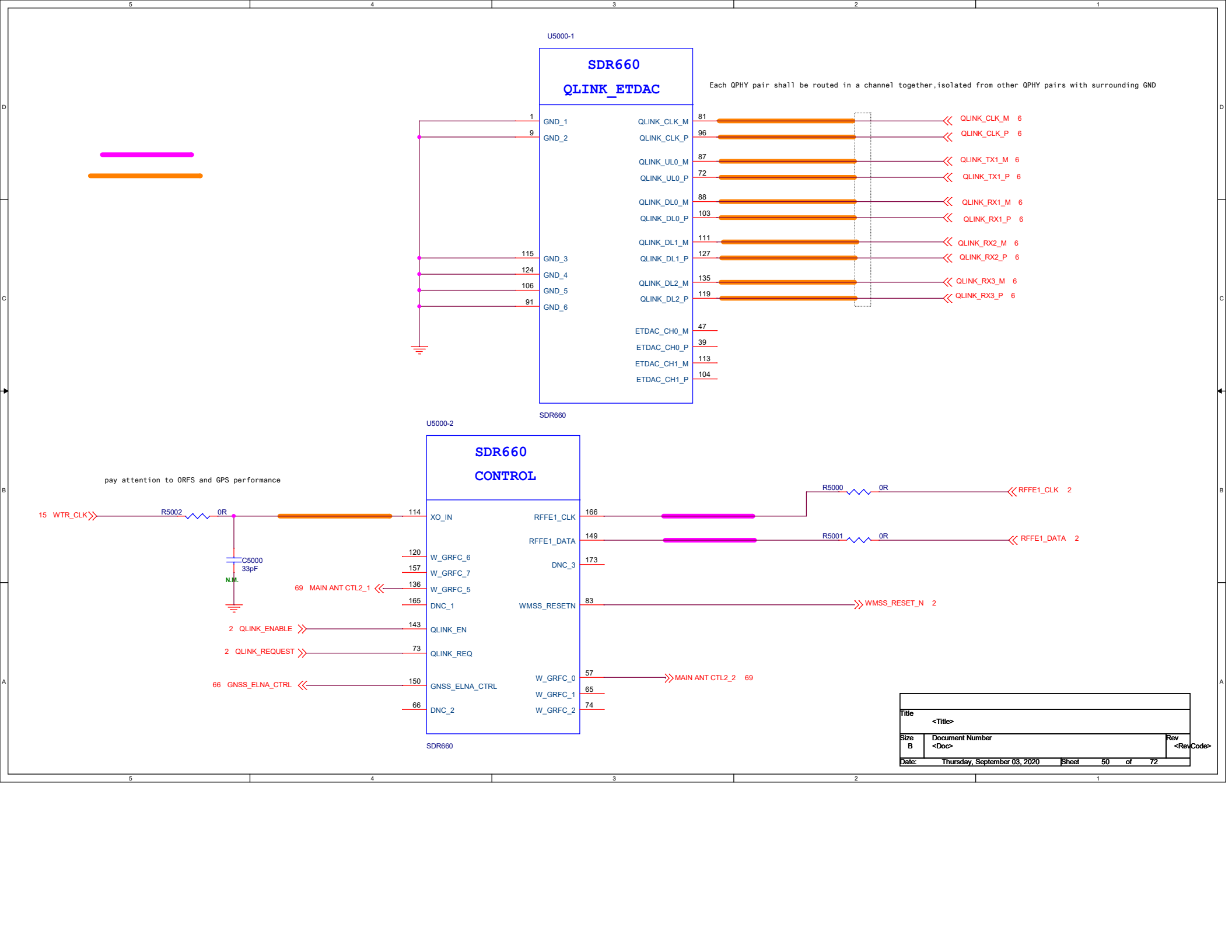


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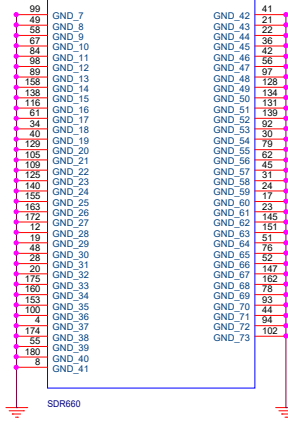
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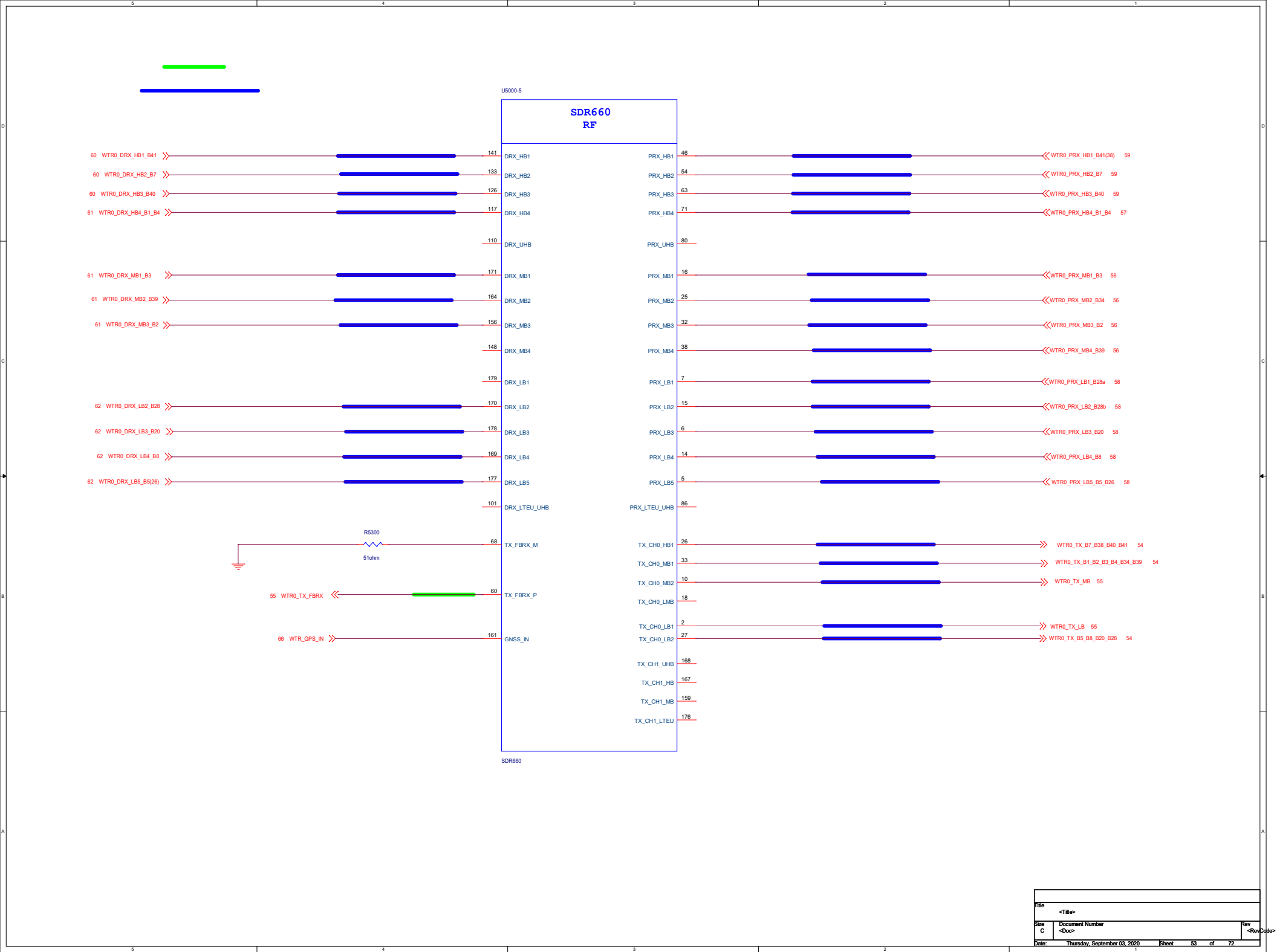


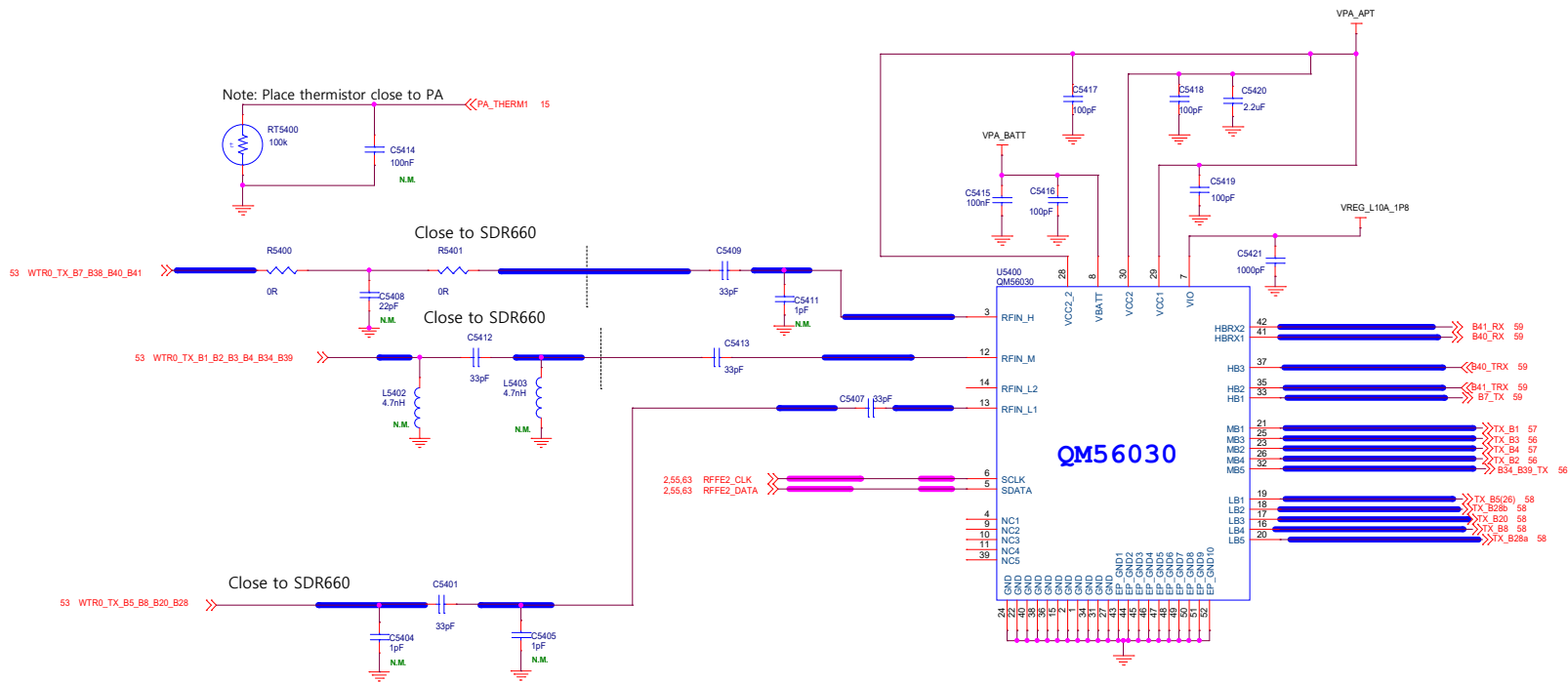


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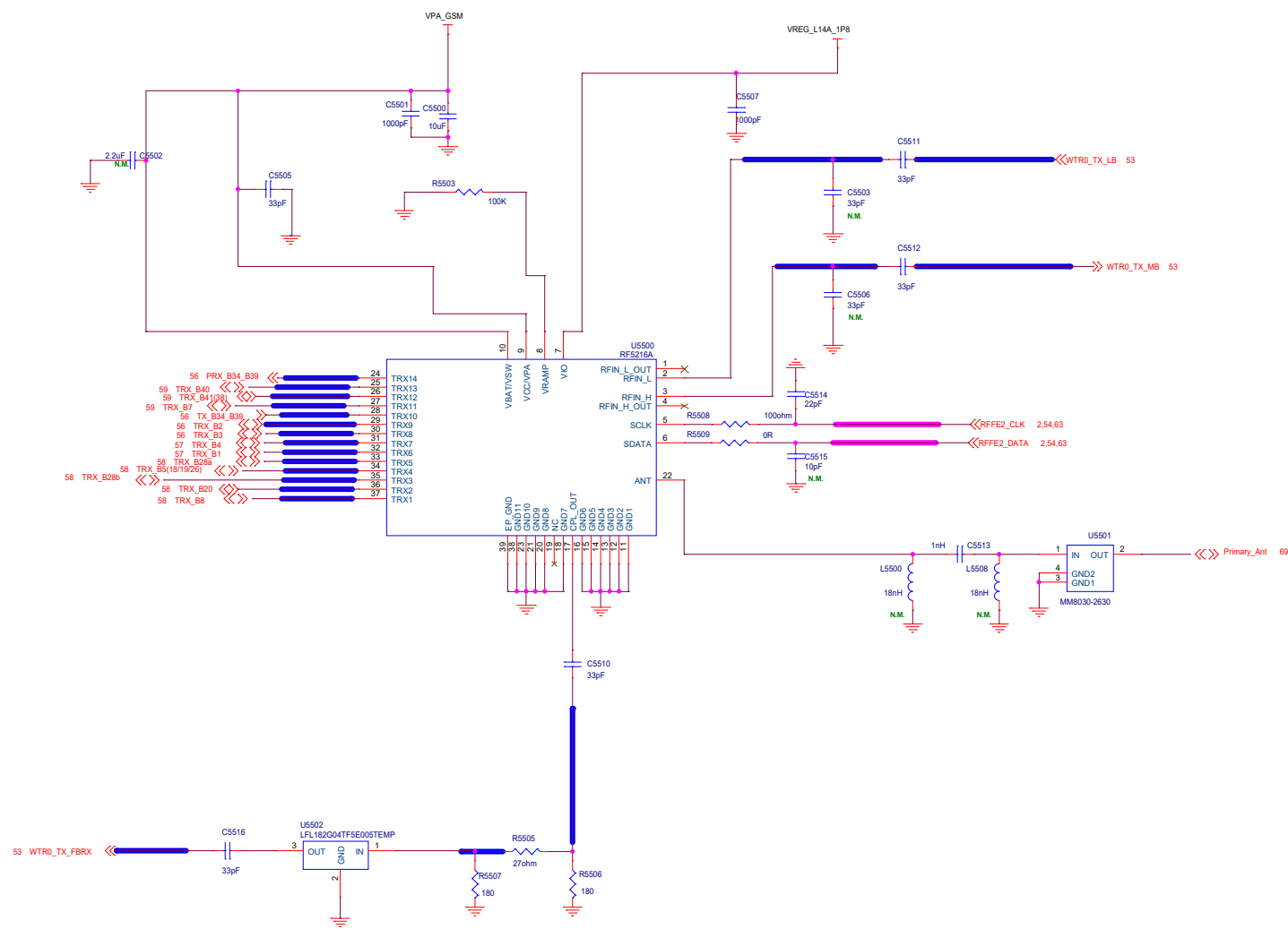
SDR660
GND





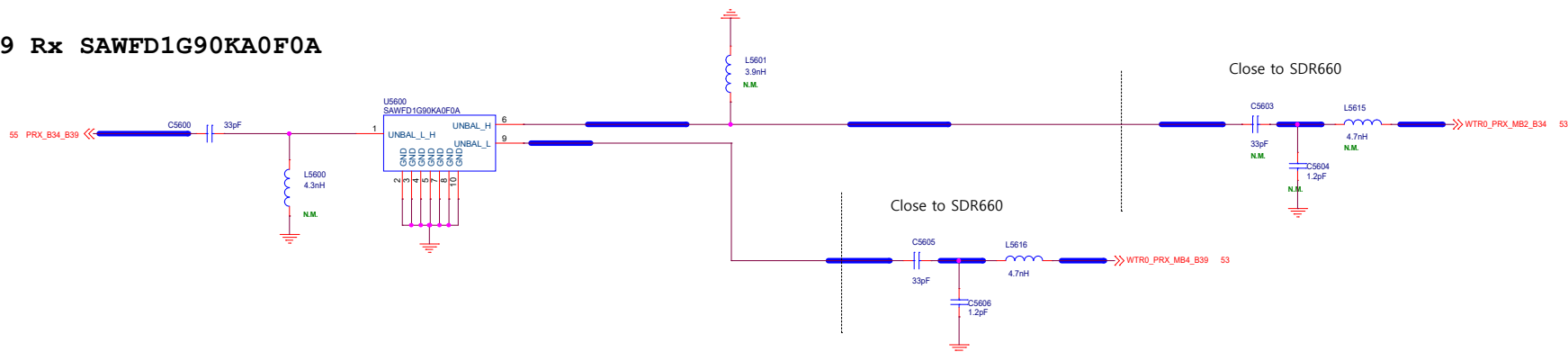


traces must be routed as a 50Ω controlled impedance

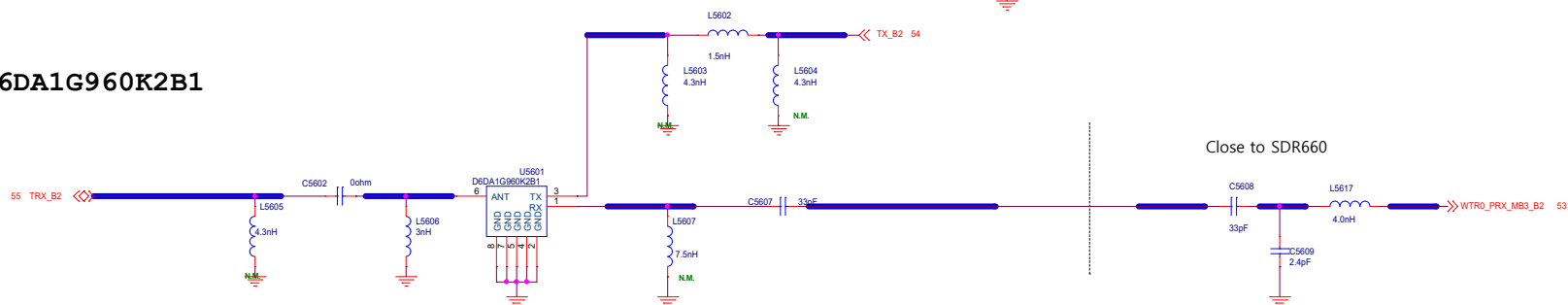


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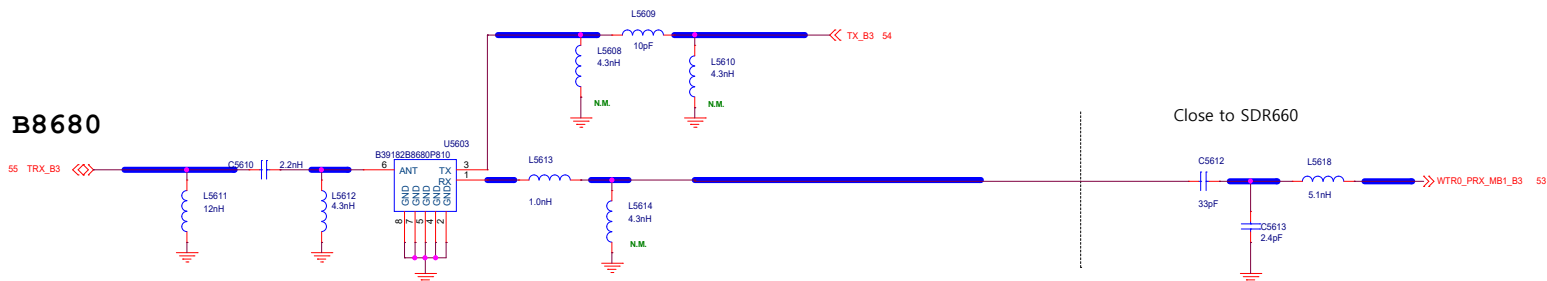
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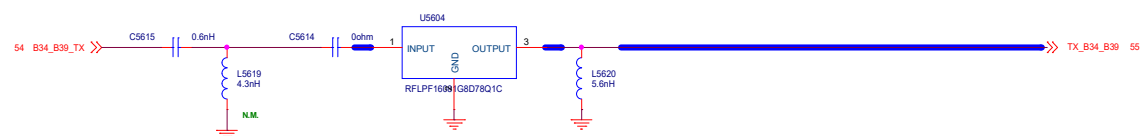
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B3 B8680

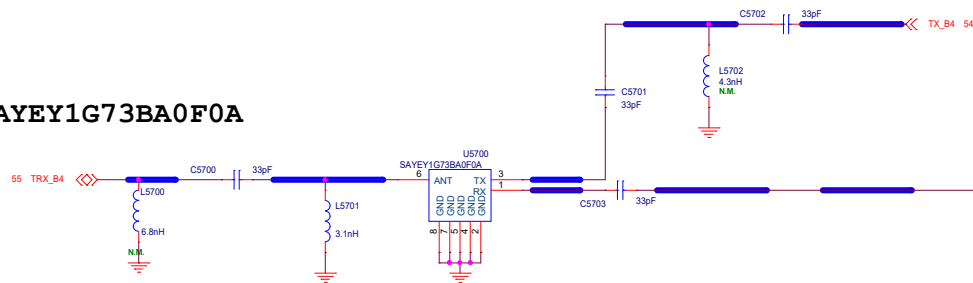


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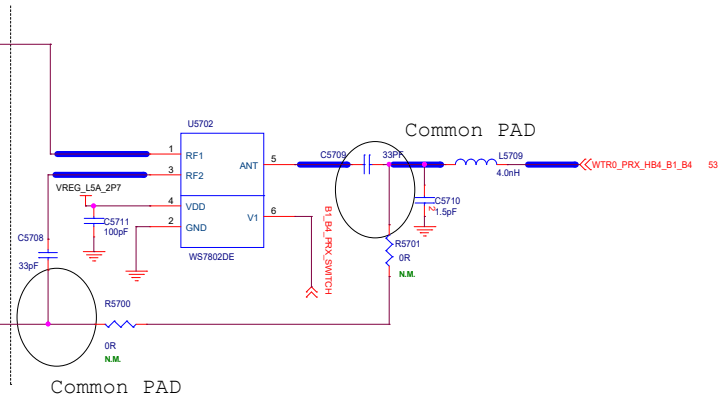
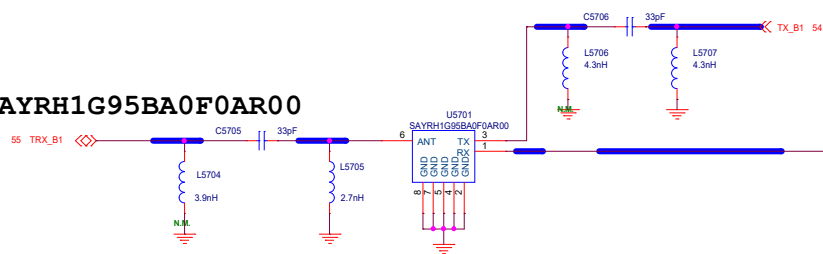


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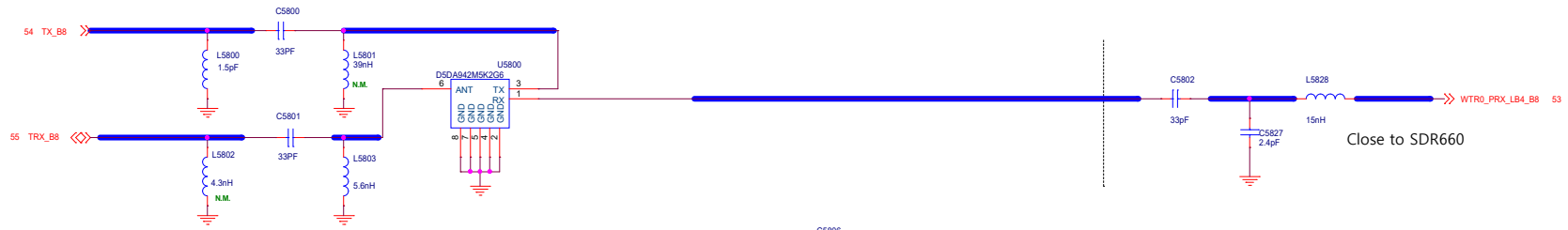


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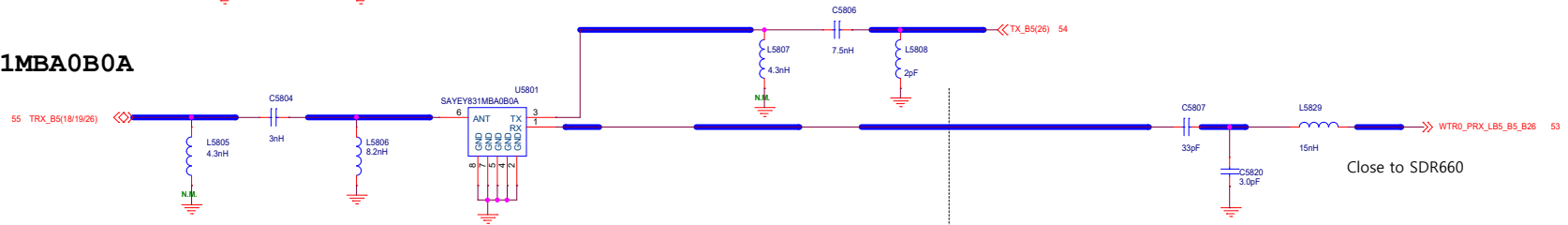


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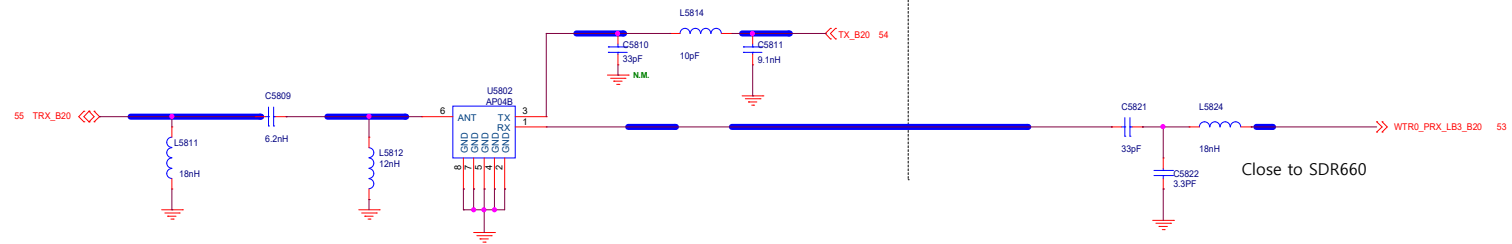
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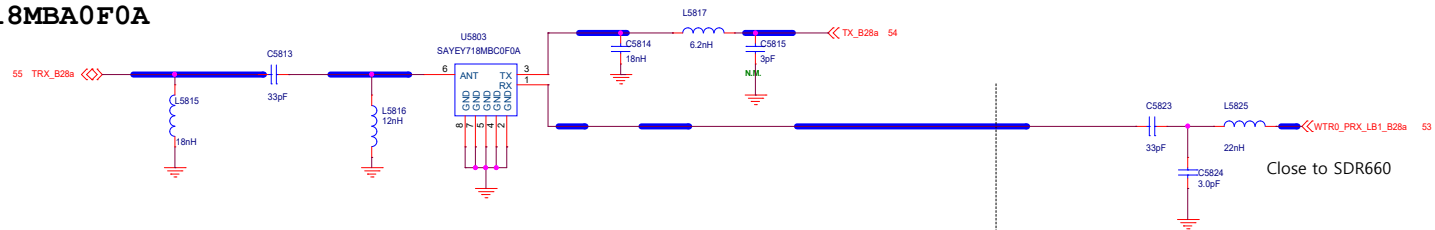
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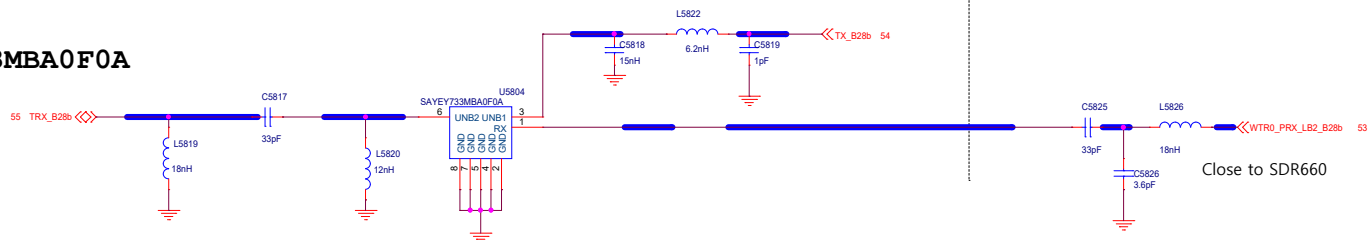
B20 AP04B



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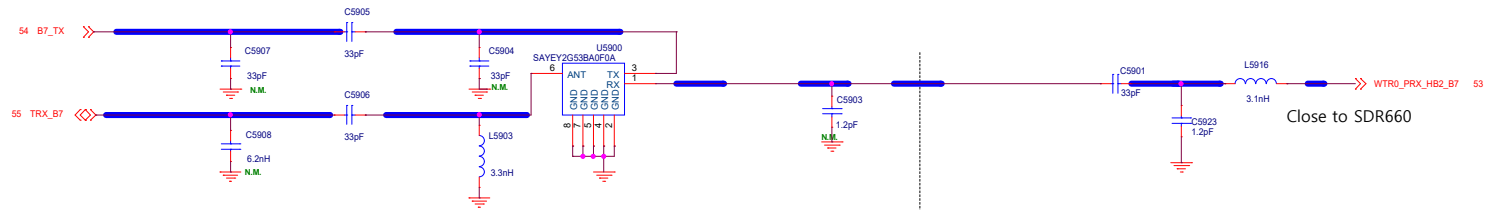


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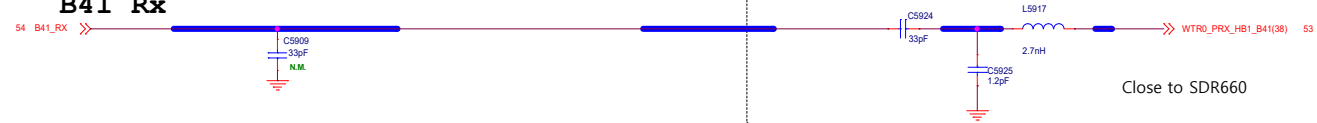


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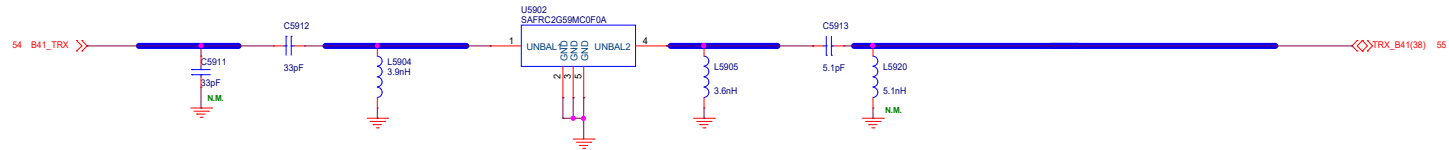
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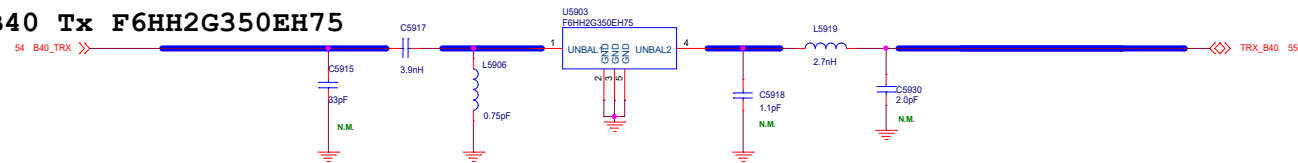
B41 Rx



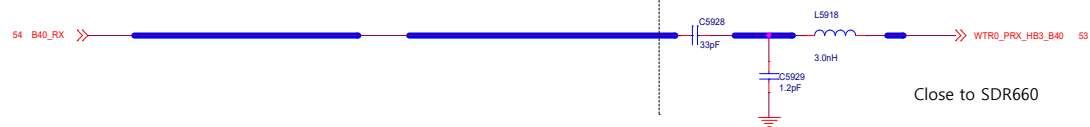
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B40 Tx F6HH2G350EH75



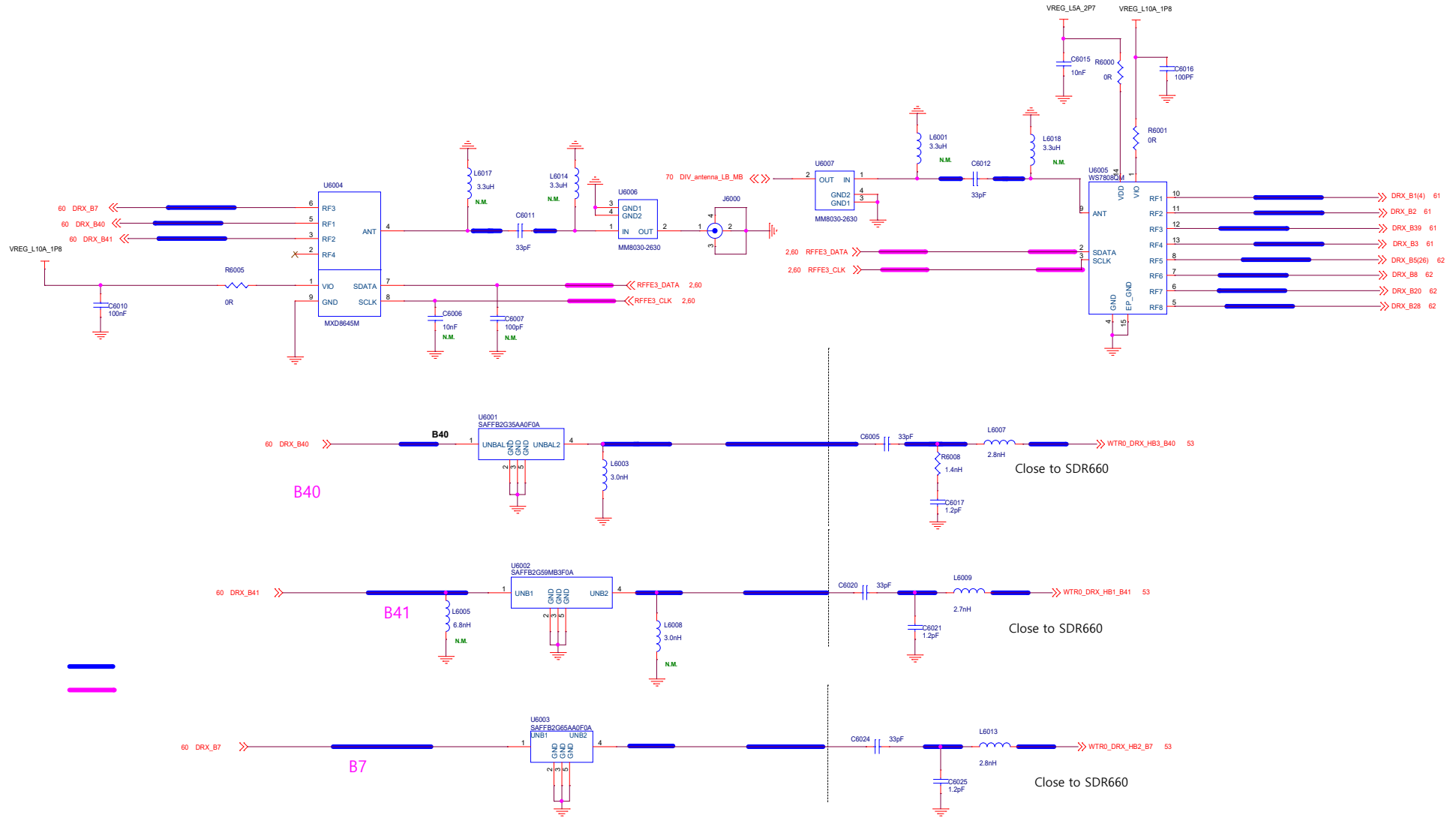
B40 Rx



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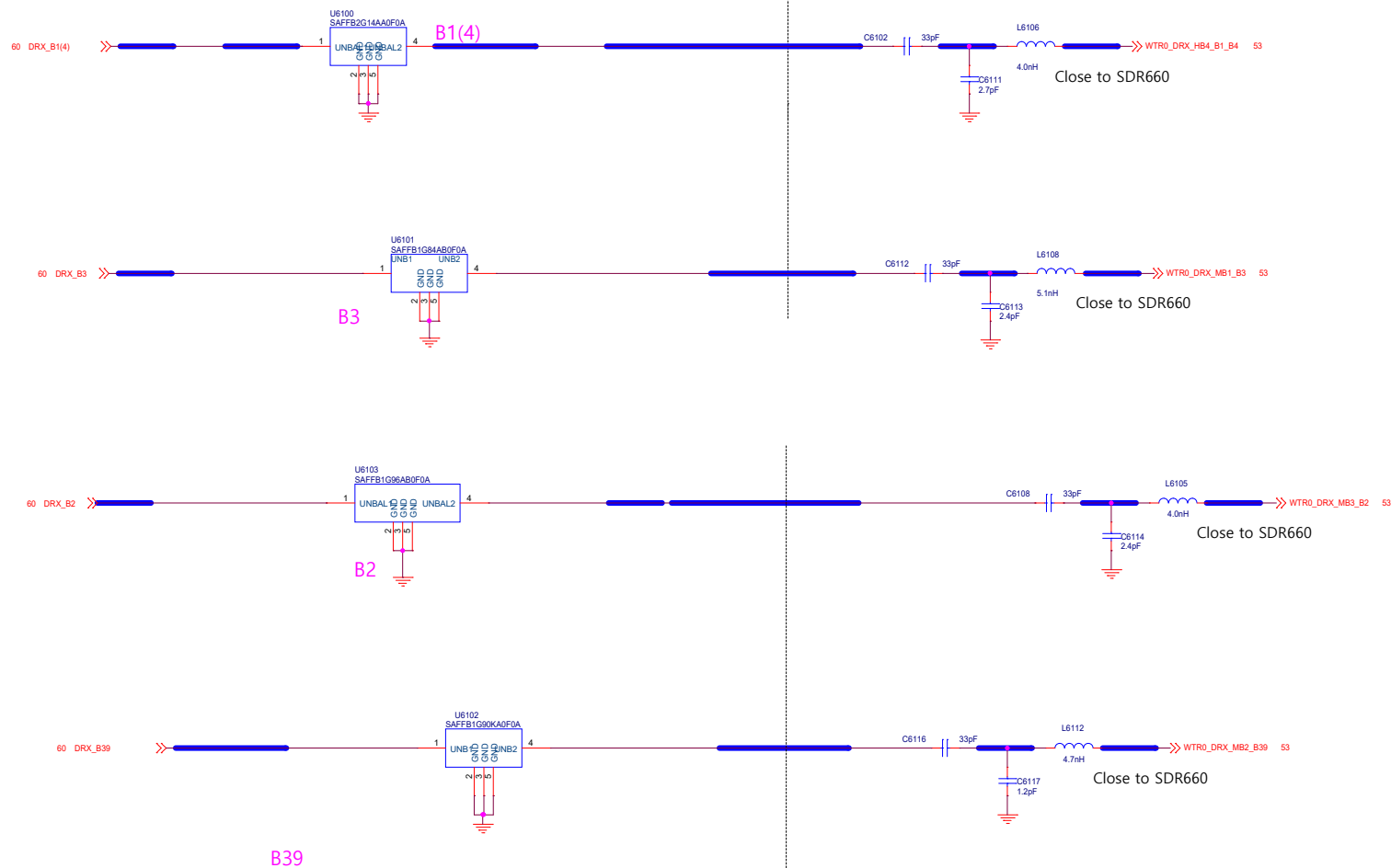
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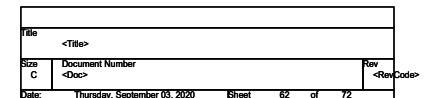
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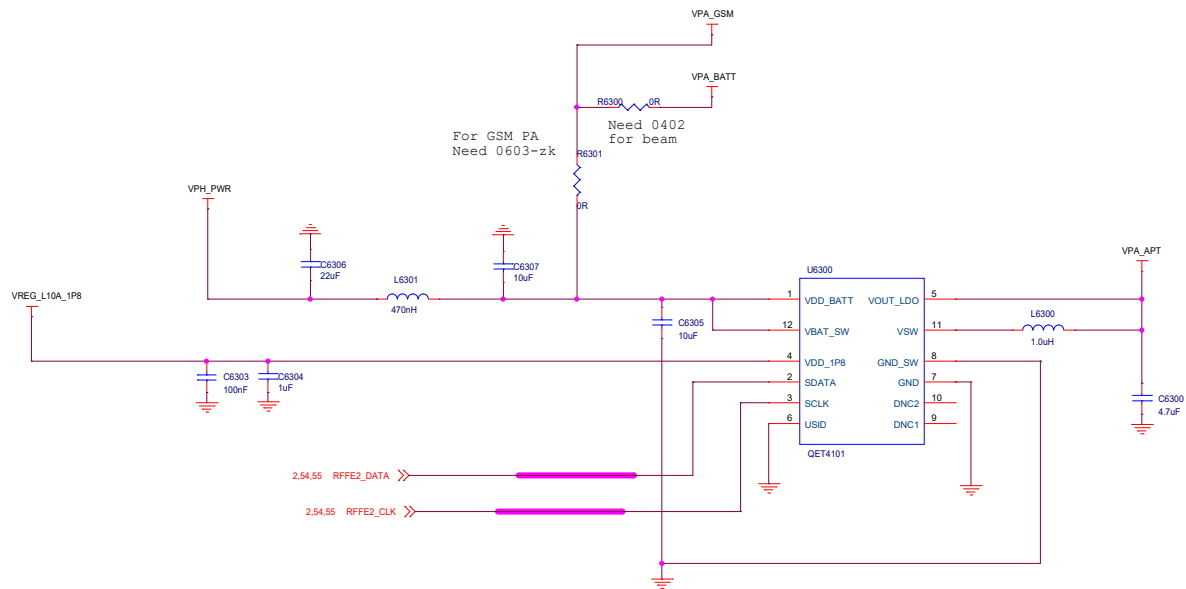


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 B1/4 Div SAFFB2G14AA0F0A
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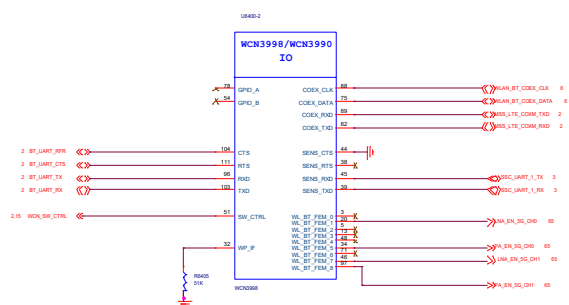
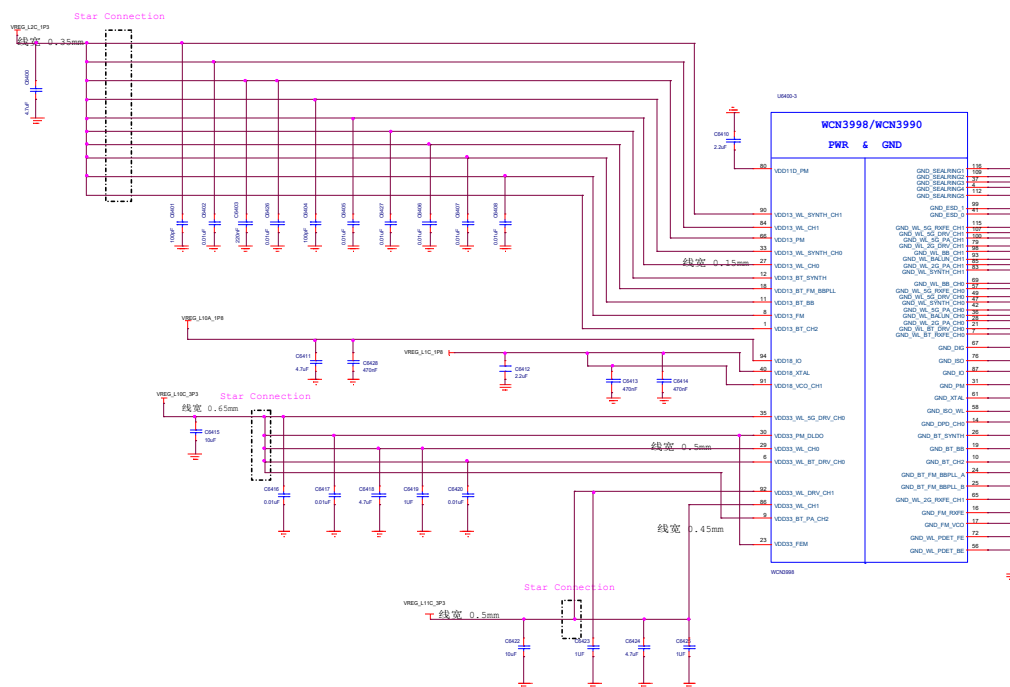
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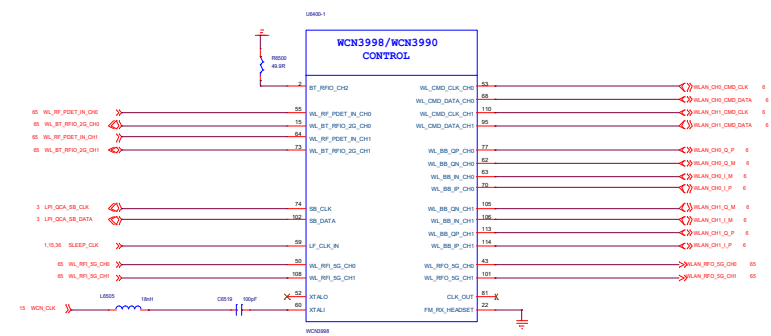
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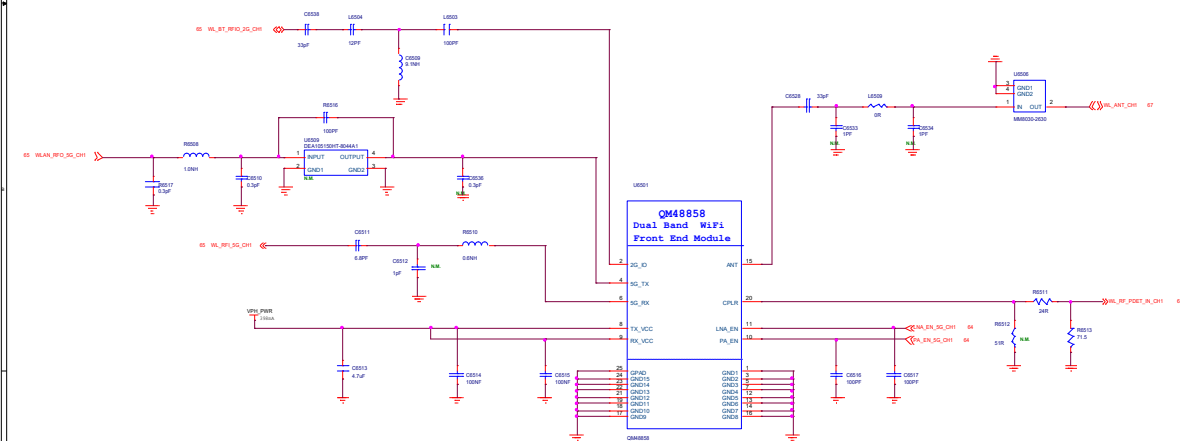


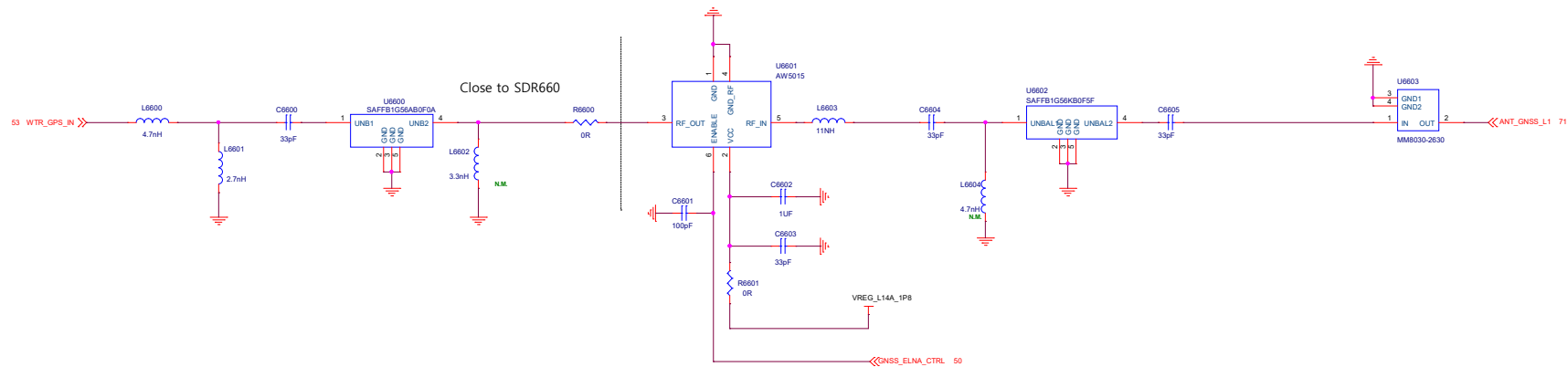
80-w1020-3 layout Guideline





80-w1020-3 layout Guideline

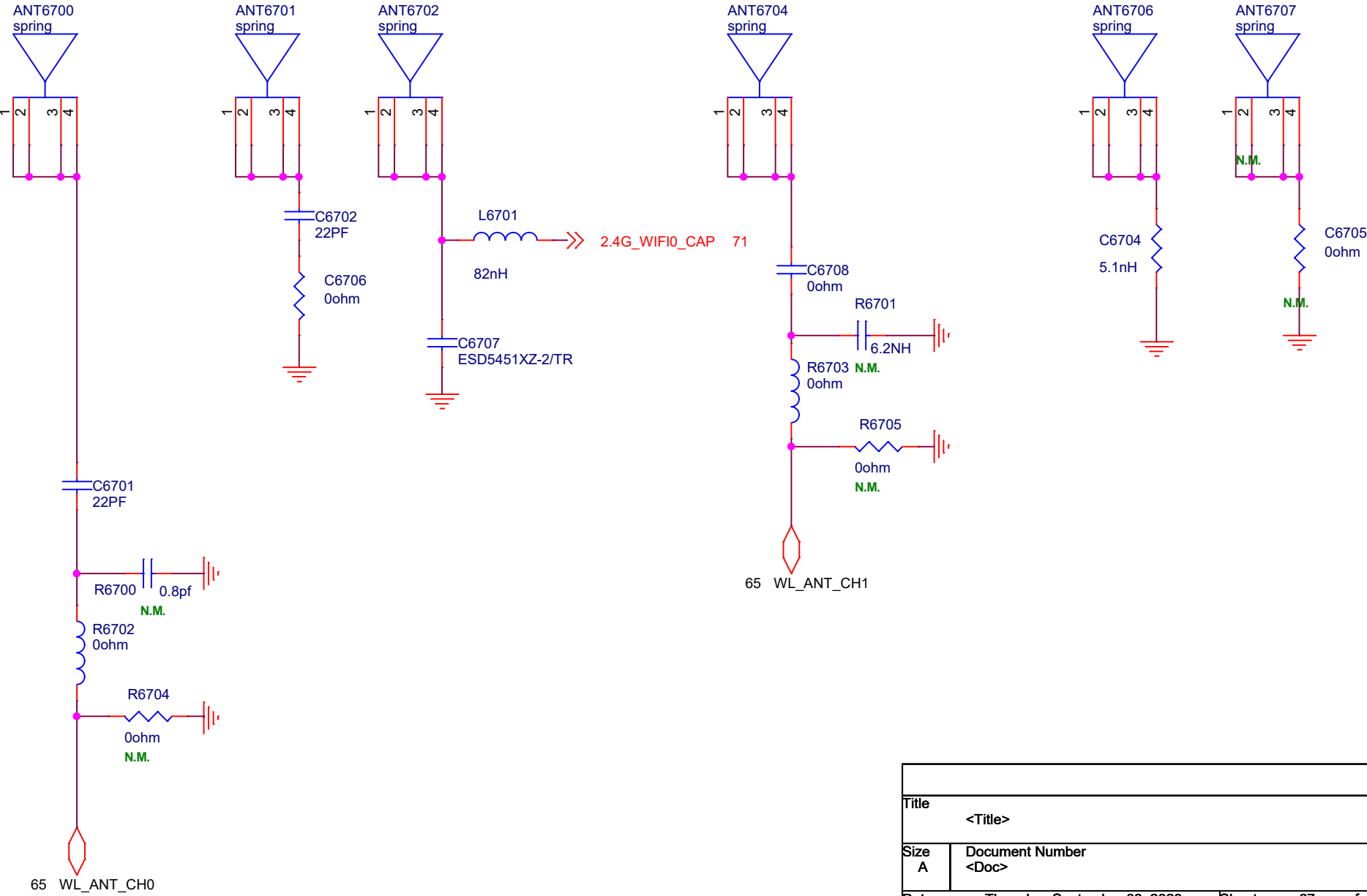




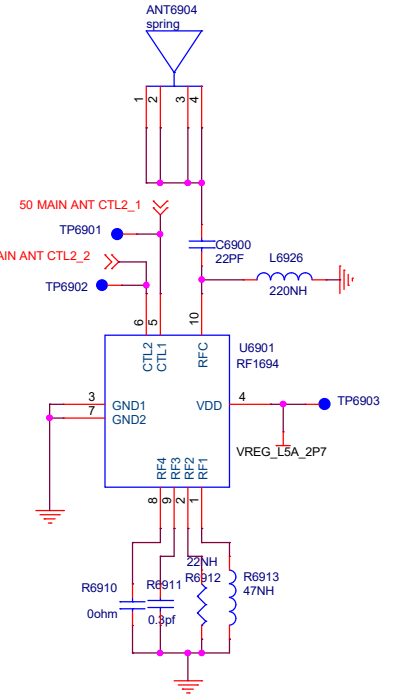
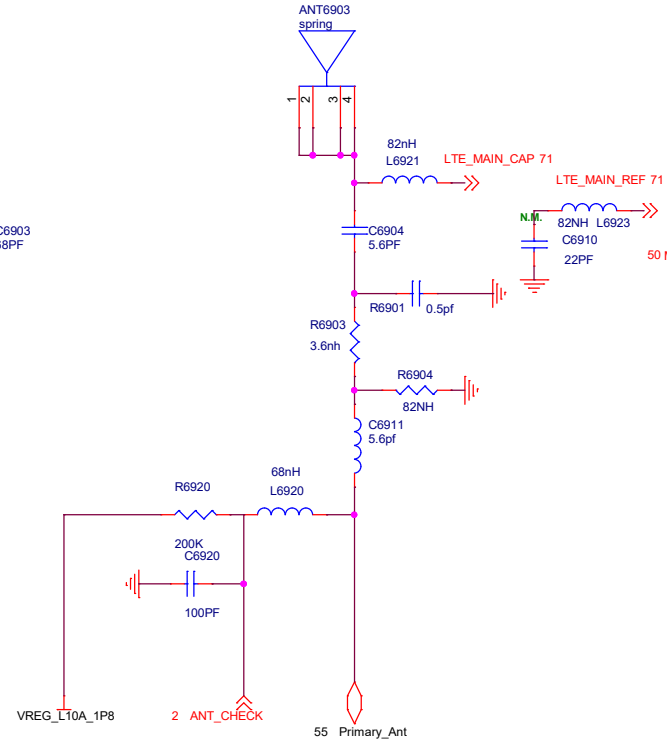
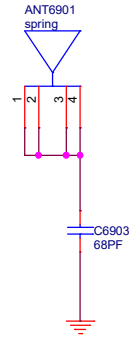
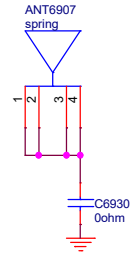
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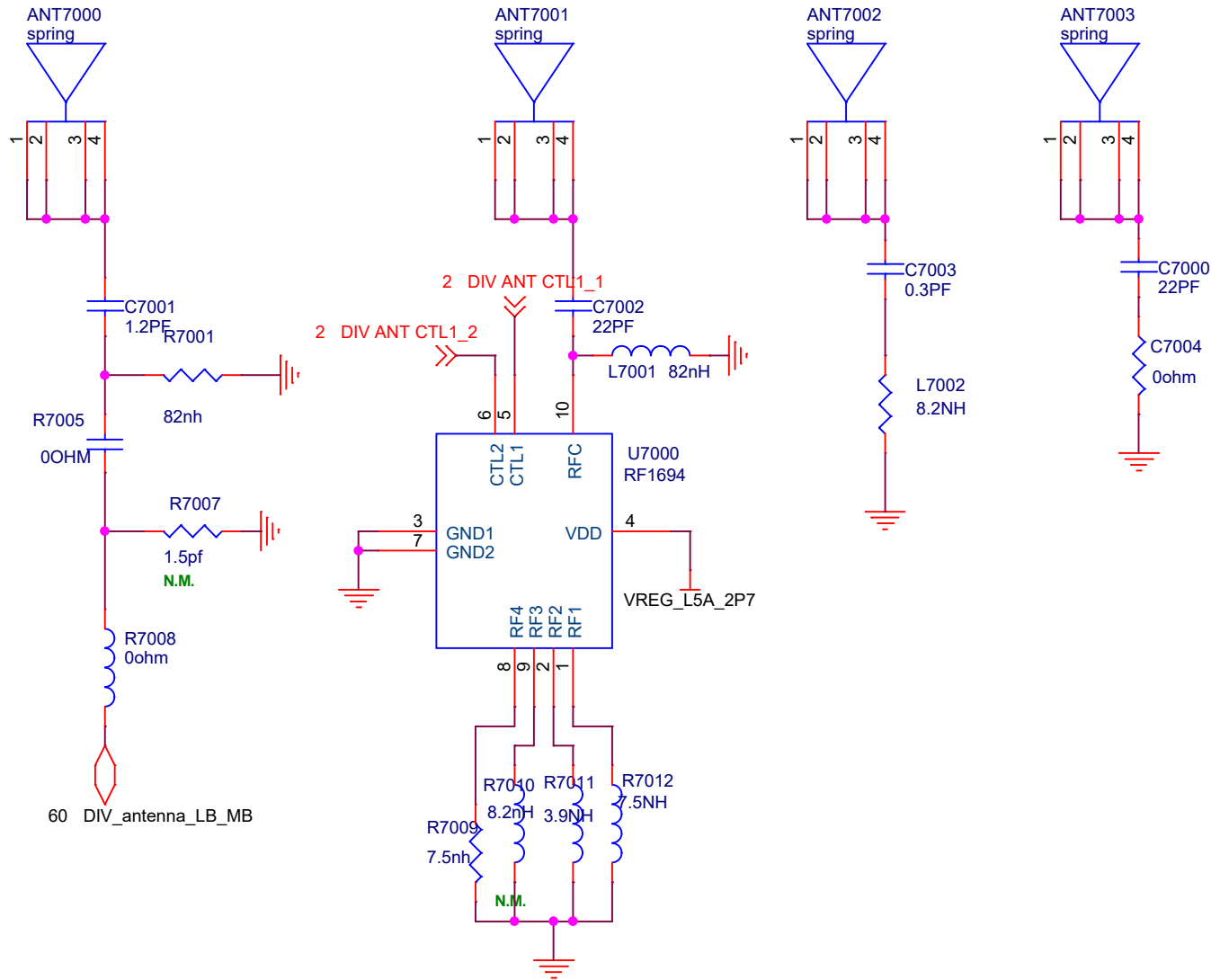


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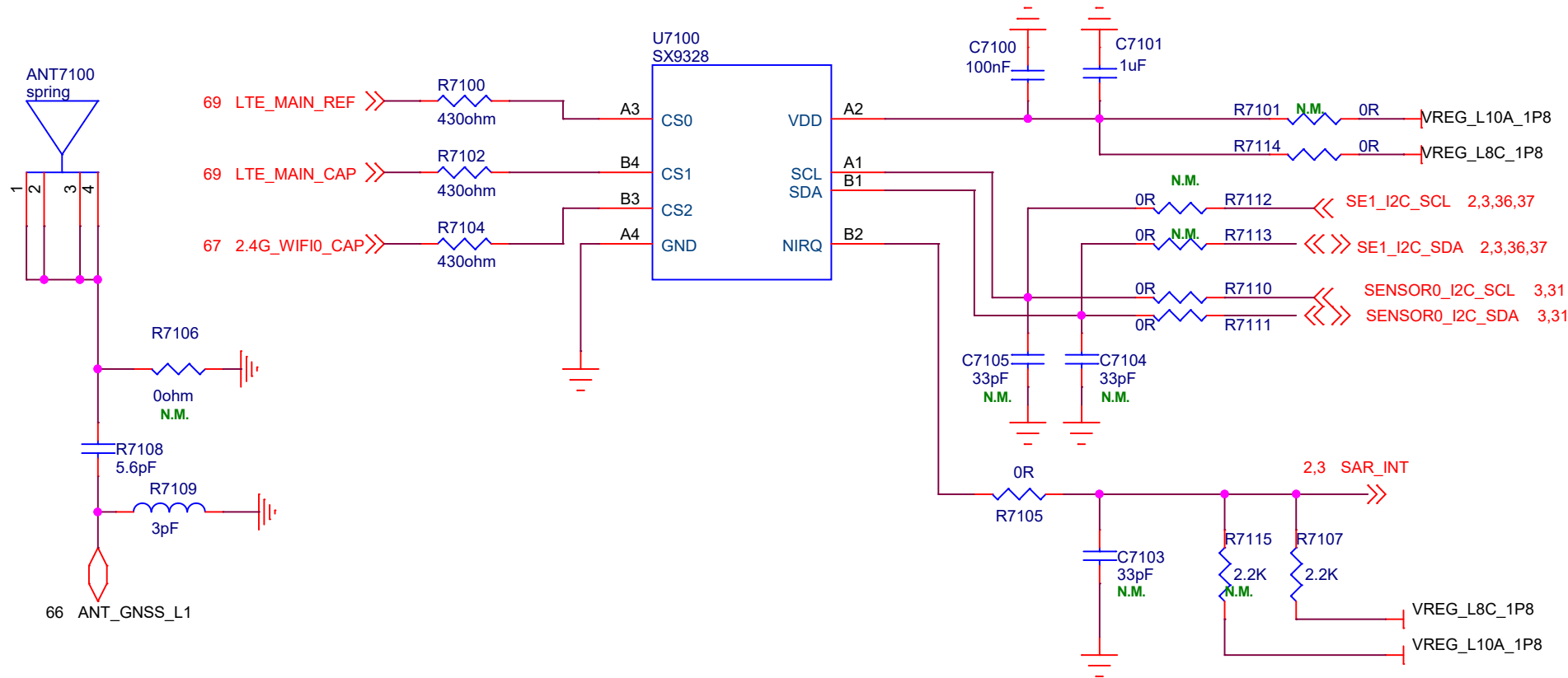
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